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The Thermal Effect of Hexagonal Boron Nitride Supports in Graphene Devices

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The Thermal Effect of Hexagonal Boron Nitride Supports in Graphene Devices

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Dedication

For my grandmother,

Fumie Hanada

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Abstract

The Thermal Effect of Hexagonal Boron Nitride Supports in Graphene Devices

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A fundamental understanding of thermal dissipation and energy transport is necessary for designing robust electronic systems and energy conversion devices. In many of these systems, minimizing the operating temperature of the working components is required for increasing the performance, lifetime, efficiency, and reliability of the device. For example, hot spots in transistors caused by the conversion of electronic energy to thermal energy has become a bottleneck in the continued scaling of microelectronics. As the demand for compact, highly conformable and mobile electronics continues to push the limit of miniaturization, these phenomena increasingly occur at the nanoscale. At these length scales, the governing physical principles differ from classical laws based on continuum mechanics and instead require a quantum mechanical treatment. The thermal transport properties of traditional three-dimensional (3D) heat conducting materials such as the metal interconnects in nanoelectronic devices tend to degrade as the critical dimension is reduced. In contrast, the thermal properties of

a new class of van der Waals-based two-dimensional (2D) materials can show different size confinement effects that can potentially be utilized for thermal management. First realized by the isolation of graphene, these materials have become attractive candidates for future-generation electronic and thermal components.

Due to their atomic thinness, the properties of 2-D materials are highly sensitive to their operating environment. The studies in this dissertation therefore aim to answer critical questions surrounding the practical applicability of graphene and its dielectric isomorph hexagonal boron nitride as thermal materials in real devices. Specifically, the fundamental heat dissipation pathways of joule-heated graphene channels are inspected within the framework of silicon-based electronics as well as next-generation flexible electronic architectures. The study reveals that lateral heat spreading is essential to mitigating hot-spot formation. As a result, the inclusion of *h*-BN as a thermal interface material between the active graphene layer and the underlying support facilitates significant reductions in device operating temperatures due to enhanced lateral heat spreading. More than a passive thermal layer, an *h*-BN support increases the intrinsic thermal conductivity of graphene relative to other support materials based on an additional study in this work. An analytical solution of the phonon Boltzmann transport equation is derived to explain the observed phenomenon.

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Chapter 1: Introduction

1.1 Background

The demand to sustain the appetite of an ever-growing energy-hungry population has been a point of international tension since the industrial revolution. In recent decades, consumer electronics and mobile computing have spearheaded global modernization. This societal advancement, however, has also come at a cost to the already strained and aging electrical grid. While data and computing can now be sent to and processed in an enigmatic cloud, the operation and maintenance of these data centers are grounded in very real, terrestrial, and highly consumptive platforms. In the U.S., energy consumption in data centers alone accounts for nearly 10% of the national electricity budget.[1] Surprisingly, approximately 50% of this energy is devoted to cooling the server racks, which has driven some companies like Microsoft to explore outlandish cooling schemes like submerging data centers to the seafloor.[1,2] In the same vein, approximately 68% of the total energy produced and consumed in the U.S from all sources is lost as wasted thermal energy.[3] As innovative as some macro-scale thermal solutions may be, such endeavors only treat the symptoms of the disease rather than the cause. To truly mitigate large thermal energy waste, attention must be focused at reducing the effects of thermal dissipation at its point of generation.

As the dimensions of electronic chips continue to shrink, the packing density of transistors has already exceeded 93 million units per mm^2.[4] As the transistor density continues to rise, the dissipated power density scales proportionally. As a result, thermal management of highly localized, nanometer-scale heating has become a grand challenge

in silicon nanodevices. Unfortunately, the physical dimensions of these devices have now become comparable to the characteristic length scales of the thermal carriers in metal interconnects that conduct the heat away from the local hot spots. For example, the room temperature thermal conductivity of copper is reduced from ~350 W m^{-1} K^{-1} at 200 nm film thickness to ~110 W m^{-1} K^{-1} for a 20 nm thick film.[5] Similarly, the semi-empirical phenomenological transport laws such as Fourier's law of conduction at the macro-scale no longer apply for treating the nanoscale geometries of contemporary electronic devices. An intense research effort is therefore underway to discover the mechanisms that fundamentally describe thermal behavior at the atomic scale and to identify a new class of electronic and thermal materials able to persist under extreme geometric confinement.

Graphene has recently been investigated as a potential solution to the thermal management issues plaguing current electronics. With an intrinsic room temperature thermal conductivity (κ) of 2000 – 4000 W m^{-1} K^{-1}, graphene's κ places it among the best heat conductors of all known materials.[6] Furthermore, graphene is only one atom in thickness and exists as a truly two-dimensional material with high electron mobility, optical transparency, and mechanical flexibility. Due to this unique combination of electronic functionality and physical robustness, graphene also has the potential to enable transformative flexible electronic devices. The substrates for such flexible device platforms however are typically material derivatives of glass or plastics with significantly lower thermal conductivity than silicon, which further constricts the thermal dissipation bottleneck.

A drawback to graphene's atomic thickness is its susceptibility to extrinsic influences. Many of its celebrated intrinsic properties only apply to the specific case

where graphene is suspended and free from any physical interface, which is an unrealistic configuration for any real-world application. Therefore, one barrier to the practical use of graphene is its tendency to underperform when it is in contact with another material. For example, due in large part to its historic use in modern electronics, SiO_2 is commonly used as a support material for graphene. Compared to the performance of free-standing graphene, however, electronic transport is found to be significantly impeded in the support architecture due to strong electron scattering caused by surface roughness, trapped charges and impurities, and surface optical phonons in the underlying oxide.[7–9] To this end, a major research effort was invested in discovering a compatible substrate for graphene, from which hexagonal boron nitride (*h*-BN) was identified as a more ideal support than SiO_2.

As an electrically insulating isomorph of graphene, *h*-BN is made of alternating boron and nitrogen atoms in place of the carbon atoms in a graphene lattice. Of greatest importance as a counterpart to graphene is its atomic flatness, chemically inert composition, and strong in-plane covalent bonds that result in a charge and dangling bond-free surface.[10] Compared to a SiO_2 support, an *h*-BN support was seen to increase the electron mobility of graphene by nearly an order of magnitude, increase the magnitude and reduce the width of the peak electrical resistivity of graphene due to reduced electron-hole puddles and carrier inhomogeneity, move the charge neutrality point close to 0 V gate voltage, boost the Seebeck coefficient, and sharpen the Seebeck polarity inversions.[10–13]

Analogous to electronic transport, supporting substrates also affect thermal transport in graphene. For example, the thermal conductivity of graphene supported on

SiO_2 was suppressed by a factor of 3-5 compared to suspended graphene.[14] This suppression reduces the utility of graphene as an effective heat spreader to mitigate thermal hot spots. As was the case for charge carriers, it has become imperative to find a suitable support that does not reduce the basal-plane thermal conductivity of graphene. The successes of *h*-BN as an ideal dielectric spurred interest in its potential as a thermal substrate as well. In contrast to the extensive studies in the literature on the electronic effect of *h*-BN in graphene, however, less focus has been paid to the thermal aspect of the graphene/*h*-BN heterostructure. In addition to its own high in-plane thermal conductivity of 200-300 W m^{-1} K^{-1} at room temperature, its similar phonon dispersion to graphene has led to speculation that the material could also preserve the intrinsic thermal conductivity of suspended graphene. While theoretical calculations have predicted such an outcome, no experimental data have been found in the literature.[15–18]

The studies in this dissertation aim to answer several of the outstanding questions surrounding the practicality of graphene heat spreaders in contemporary and future flexible electronic devices as well as the fundamental role of the support substrate on its dominant thermal energy carriers.

1.2 Scope of Work

This dissertation includes three experimental studies on the thermal properties of graphene and how they can be modified by interactions with various supporting structures. The first two studies use a scanning thermal microscopy technique to produce thermally mapped images at the nanoscale while the third study uses a suspended micro-heating device to measure the thermal conductivity of *h*-BN encapsulated graphene.

The first study is presented in Chapter 2 and addresses a basic question that is imperative to thermal design, but has been largely brushed aside in the literature. Through experimental, analytical, and numerical methods, a comparison between the substrate-dependent thermal benefits of increasing graphene's κ_{gr} versus increasing its interfacial thermal conductance, G, is drawn. These two parameters represent two parallel pathways for heat transfer: laterally across the sample and longitudinally into the underlying substrate. Unveiling of the dominant thermal pathway leads to rational thermal design of graphene-based electronic devices. It was found that for thermally thick platforms where the interface resistance was much smaller than the spreading resistance of the substrate, increasing the effective thermal conductivity, κ, is more important than G.

Based on the results of Chapter 2, it is imperative to increase the effective lateral thermal conductance for the graphene layer to reduce the operating temperatures in thermally thick flexible substrates. However, many of the attractive electronic properties of graphene, such as its high electron mobility, are reduced when chemical modifications are made to enhance its thermal properties. Instead, Chapter 3 investigates the use of hexagonal-boron nitride (*h*-BN) as an interfacial heat-spreading layer between the graphene and substrate. Scanning thermal microscopy is used to determine the comparative effect of introducing *h*-BN as a heat-spreading layer on two representative substrates: 300 nm SiO_2 on silicon and 100 μm flexible Dow Corning Willow Glass (WG). The theoretical framework derived in Chapter 2 is modified to include the different thermal behaviors of the silicon and WG substrates and agrees well with the experimental findings.

Chapter 4 presents a fundamental experimental study of thermal transport in graphene/*h*-BN heterostructure to uncover the role of the substrate in phonon transport. A suspended micro-heater device is fabricated to measure the thermal conductivity of multi-layer graphene sandwiched between two *h*-BN sheets. The results are compared to oxide supported and oxide encapsulated multi-layer graphene and reveal that *h*-BN is a superior thermal support for graphene. A theoretical analysis based on the Boltzmann Transport Equation (BTE) in the relaxation time approximation is derived to show that even for atomically smooth interfaces, SiO_2 more strongly suppresses phonon transport than *h*-BN.

Chapter 2: Effects of Basal Plane Thermal Conductivity and Interface Thermal Conductance on the Hot Spot Temperature in Graphene Electronic Devices*

2.1 Introduction

Because of its high intrinsic electron mobility, mechanical strength, optical transmission, and thermal conductivity, the envisioned uses for graphene have grown rapidly since its successful exfoliation just over a decade ago.[19–21] In particular, graphene has been explored for use in electronic devices fabricated on not only silicon but also flexible substrates due to the unprecedented electronic properties and mechanical flexibility of the two-dimensional (2D) material.[22] While thermal management of silicon nanoelectronic devices has remained a significant challenge due to the high power density and operating temperatures, [23,24] similar challenges have emerged for graphene electronic devices. For example, thermomechanical failures have already been observed in flexible graphene electronic devices due to the low thermal conductivities and glass transition temperatures of most flexible substrates.[22,25,26] The high basal-plane thermal conductivity of graphene has been explored to address this and other challenges in thermal management.[27,28] However, it remains unclear whether the high basal-plane thermal conductivity of graphene can lead to an added benefit of enhanced heat removal and reduced peak temperatures during operation since it is only one atom thick.[25] Because of the high surface to volume ratio of graphene, it is uncertain whether the hot

* The content of this chapter was published in D. Choi, N. Poudel, S. Cronin, L. Shi, "Effects of basal-plane thermal conductivity and interface thermal conductance on the hot spot temperature in graphene electronic devices", Applied Physics Letters, **110**, 073104 (2017). The sample was fabricated by N.P. and S.C., D.C. carried out the measurements and analysis, L.S. designed the experiment and contributed to the thermal measurements and data analysis.

spot temperature is more sensitive to the thermal interface conductance (G) between the 2D atomic layer and the substrate than to the in-plane thermal conductivity (κ).[6,25]

In addition, physical defects such as rips, tears, and wrinkles are often introduced during the fabrication of these devices and can potentially result in local hot spots during operation.[29–32] Such hot spots in turn can significantly degrade performance and reliability and are typically on the micron to submicron scale. In recent years, the popularity of optical thermometry methods to study thermal transport in low-dimensional materials has grown due to their speed and ability to non-invasively probe large areas.[33–36] For example, Raman spectroscopy has been used to determine the thermal conductivity of suspended graphene by tracking the shift in Raman active phonon modes, typically the 2D and G peaks, or the ratio between the two. However, the lateral resolution of these methods is fundamentally limited by the diffraction limit of the wavelength of light used, which is typically on the scale of several hundred nanometers. Shifts in the 2D or G peak are also not very sensitive to temperature and typically require large heating powers to accurately detect changes in temperature, which limits the temperature sensitivity of the technique to about 50 K.[37–41] Furthermore, due to uncertainties in temperature and the absorbed laser power in the graphene, studies conducted using similar measurement schemes have resulted in a wide variability in the reported thermal conductivity of suspended single layer graphene from as low as 600 W m^{-1} K^{-1} to as high as 5000 W m^{-1} K^{-1}.[33–36] Since defects in graphene are typically below 100 nm in the lateral dimension and may cause a temperature rise of only a few degrees Kelvin above ambient at low power dissipations, high-resolution thermal imaging is essential for visualizing sub-micron hot spots in the study of thermal reliability in electronic devices. To this end, we

employ electrostatic force microscopy (EFM) and scanning thermal microscopy (SThM) techniques to identify defects at the nanoscale in a graphene electronic device and analyze their effect on thermal performance. A numerical electro-thermal analysis is further employed to correlate the measured hot spot temperature with the basal-plane thermal conductivity and the interface thermal conductance of graphene. In addition, an analytical model is coupled with numerical simulations to determine the effects of graphene thermal conductivity or interface thermal conductance enhancement on the hot spot temperature.

2.2 Scanning Thermal Microscopy and Electrostatic Force Microscopy

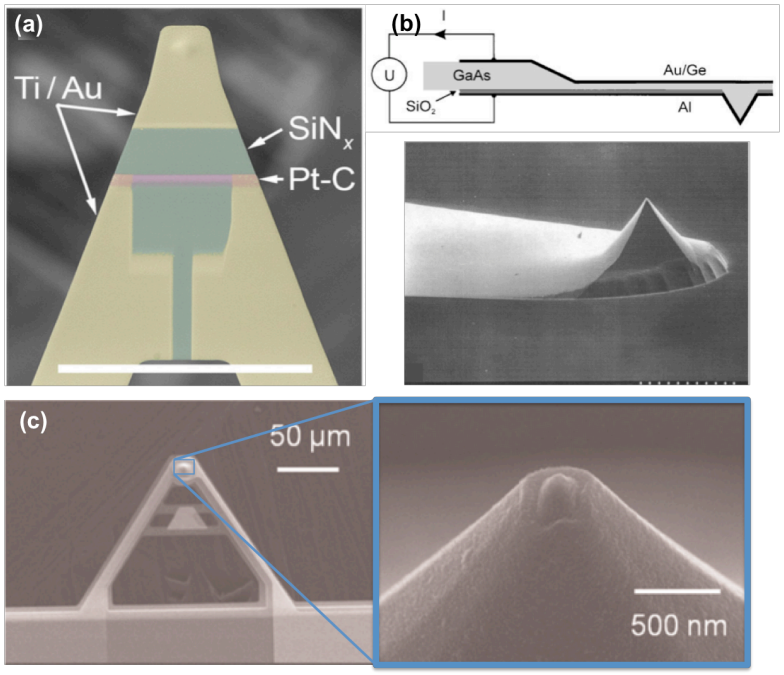

Figure 2.1: Variations of SThM probes. (a) Resistor thermometer based tip.[42] (b) Schottky Diode based thermal sensor.[43] (c) Thermocouple temperature sensitive element.[44]

Scanning thermal microscopy is a modified atomic force microscopy technique whereby a temperature sensitive element is fabricated on or near the apex of an AFM tip. Many SThM techniques have been conceived,[45] each varying in experimental implementation. Some measure the signal from an electro-thermal sensor,[44] while others measure temperature indirectly via thermal expansion of the sample or a polymer capping layer.[46,47] The configuration of the temperature sensitive element at or near the tip itself is also different between different experiments. For example, one type of the temperature sensor is the resistive thermal detector (RTD) shown in Figure 2.1(a). In this design, a thin Pt-C resistor was deposited via Ga^+ focused ion beam (FIB) on the end of a V-shaped SiN_x cantilever, which acted as the temperature sensitive element. As the tip scanned over the heated sample, the change in resistance of the RTD was tracked and used to generate a thermal image.[42] In a different design, shown in Figure 2.1(b) a Schottky diode was created by deposition of a thin layer of aluminum on the tip of a GaAs tip and cantilever.[43] Since the I-V characteristics of the junction are sensitive to temperature, a thermal image is produced by tracking the bias required to maintain a constant forward current.[43] Another commonly adapted SThM tip configuration is the thermocouple junction based tip, where a thermocouple is fabricated directly on an AFM tip by subsequent evaporation of two dissimilar metals, as shown in Figure 2.1(c).[48] Unlike the working principles for the Schottky Diode and RTD variants, however, the thermoelectric effect persists with the continuous down-scaling of the thermocouple junction. As a result and despite the difficulty in probe fabrication, the thermocouple junction design has been increasingly adopted due to its accuracy and potential for enabling nanometer scale thermal resolution. With this type of detector, as the tip scans across a heated surface the

measured thermoelectric voltage generated by the temperature rise at the tip-sample contact provides a thermal map simultaneously with the topographical map. Under ideal measurement conditions the thermocouple-based SThM technique can theoretically enable thermally resolved features down to ~10 nm, limited mainly by the tip-sample contact area.[44] In the past few decades since SThM's inception, however, it has been shown that achieving such ideal conditions is not straight forward since the thermal signal is highly susceptible to thermal contamination when the measurement was conducted in atmosphere. To this end, the following section outlines some of the factors that distort the true thermal field of the sample and a few different approaches used to eliminate them.

2.2.1 Distortions in SThM Measurements and the Double Scan Technique

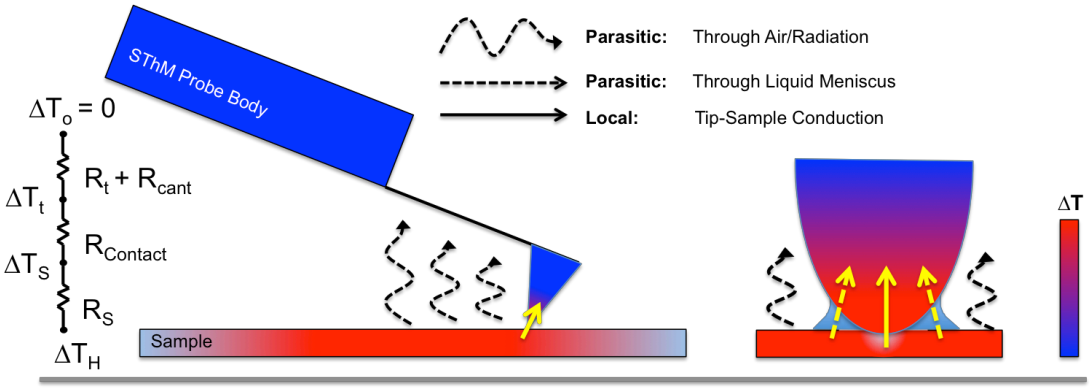

Figure 2.2: Parasitic heat transfer between the sample and probe cause distortions in the signal.

In general, a good quality SThM measurement is characterized by 1) minimal disturbance to the thermal field being measured, 2) a highly sensitive thermal response of the tip to a thermal gradient and 3) a truly localized signal free from thermal distortion. The first two goals are pursued through careful design of the probe. In the thermal circuit

shown in Figure 2.2, ΔT_H, ΔT_S, ΔT_t, and ΔT_o are the true temperature of the sample, the temperature of the sample at the surface, the measured temperature of the thermocouple tip, and ambient temperature, respectively and R_s, $R_{contact}$, and $R_t + R_{cant}$ are the spreading thermal resistance of the sample, the thermal contact resistance between the sample and tip, and the thermal resistance of the conical tip and cantilever, respectively. According to this simple circuit, increasing the probe thermal resistance relative to the tip-sample contact resistance minimizes the temperature drop across the contact for any given heat flux, Q_{tip}, into the tip. As a result, the thermal sensitivity of the tip, which is defined as the temperature rise in the tip per degree temperature rise of the sample, is increased. Furthermore, increasing $R_t + R_{cant}$ reduces the magnitude of the heat flux from the sample into the tip and through the probe body, thereby minimizing the thermal disturbance of the tip on the true sample temperature. Mathematically, maximizing ($R_t + R_{cant}$) minimizes both $\Delta T_t - \Delta T_S$ and $\Delta T_S - \Delta T_H$. To this end, the probe used in this study was designed to meet these requirements and consists of Pt-Cr thermocouple deposited onto an SiO_2 tip attached to a long silicon nitride cantilever.[48]

The third condition for a properly designed SThM measurement requires a quantitative measurement of the local sample temperature at the tip-sample contact. The highest resolution attainable is set by the tip-sample contact area, which is limited by the radius of the apex of the tip which can be made to be as small as ~10 nm.[44] As shown in Figure 2.2, this local signal corresponds to measuring the heat transfer between the tip and sample through solid-solid conduction through the contact (solid yellow pathway). However, for measurements performed in ambient conditions, non-local thermal signals generated by parasitic pathways between the heated sample and the SThM probe are

prone to mask the desired local signal. The spatial resolution of the thermal map generated by SThM therefore depends on the relative dominance of the various heat transfer mechanisms between the heated sample and the tip. Depending on a number of experimental factors including the sample cleanliness, roughness, surface chemistry, the lateral size of the heated area, tip material, and magnitude of the sample temperature, these non-local signals can indeed dominate over the desired tip-sample contact signal. For example, when device temperatures are relatively low, it has been shown that conduction through the water meniscus that forms around the tip-sample contact can dominate over the solid-solid conduction through the contact.[26] While this effect acts to reduce R_c, it also broadens the contact area and reduces the spatial resolution. Depending on the surface conditions of the sample, the effective contact area can be as large 50 nm in the presence of a water meniscus.[44,49]

However, a much larger obstacle exists in the case of large heated areas where parasitic heat transfer via conduction/convection through the air gap between the probe and sample can contribute significantly to the measured signal. Figure 2.3 shows two thermal maps generated when (a) the tip is scanned in contact with and (b) lifted 100 nm out of contact with a 5 μm wide, joule-heated graphene channel on oxidized silicon (outlined in white dashed lines). The contribution through the air alone is seen to constitute nearly 70% of the contact-mode signal. Furthermore, thermal contamination is widespread, encompassing the full 5 μm graphene width and extending several microns outside of the channel. To achieve truly quantitative high resolution SThM scans, it is critical to remove the non-local contributions from the parasitic transport through the air. One solution is to perform the experiment in ultra-high vacuum (UHV), which eliminates

both the water meniscus and air contributions to the signal.[44] In this measurement scheme, the sample temperature is directly proportional to the thermovoltage signal collected with the tip in contact with the sample. Furthermore, it has been demonstrated that a thermal resolution down to ~15 mK can be achieved when a modulated joule-heating current is applied to the sample at frequency *f* and lock-in detection is used to detect the induced thermal signal at 2*f*.[44] Although UHV allows for an analytically and conceptually simple method to obtain quantitative and truly local temperature maps with SThM, it is experimentally complicated.

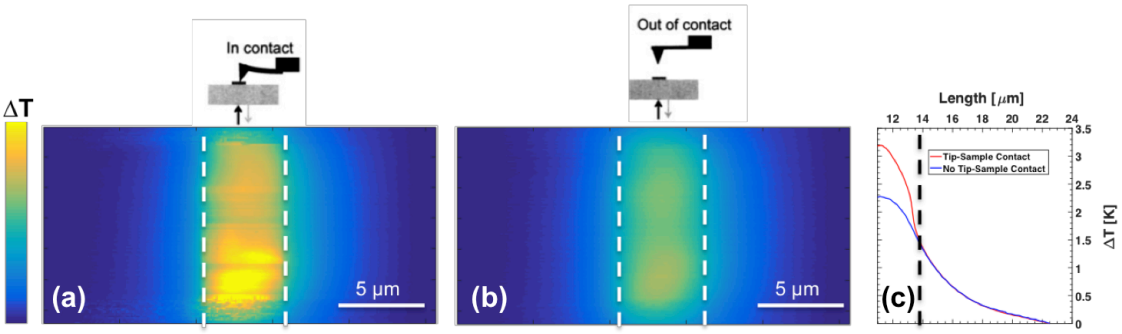

Figure 2.3: Thermal maps of a joule-heated graphene channel (outlined in white dashed lines) when the tip is scanned in (a) contact mode and (b) lift mode. A large thermal contribution via conduction/convection through the air to the measured temperature profile is visible in (b) even though there is no physical contact between the tip and sample. (c) Line scans through the center of the images in (a) and (b) show that the measured lift signal can be as much as ~70% of the total contact mode profile.

To supplant the need for specialized equipment, Kim *et al.* reported a double scan technique to enable localized, quantitative SThM applicable under ambient conditions.[50] In this method, they utilized a setting available in most commercial AFM software where the same scan line can be scanned twice, once in contact and a second time with the tip

out of contact with the sample. During the first scan, the tip profiles the surface in contact mode to obtain the sample topography and thermovoltage produced by the tip. Using the thermopower, S, of the tip, the contact-mode thermovoltage can be converted into a sensed temperature rise in the tip, $\Delta T_{t,C}$. In a second scan of the same line, the thermovoltage is recorded while the tip is lifted to a set height above the sample and traced along the stored topographic profile of the first pass. In this non-contact mode, the heat transfer through the tip-sample contact vanishes, $Q_{TS} = 0$. As such, the temperature rise in the tip, $\Delta T_{t,L}$, consists of only the contribution through the air. Analytically, Kim and co-workers solved for the relationship between $\Delta T_{t,C}$, $\Delta T_{t,L}$, and the true sample temperature, ΔT_S, by linearly combining the governing energy equations for the two scan modes and showed:[50]

$$\Delta T_S = \Delta T_{t,C} + \varphi\left(\Delta T_{t,C} - \Delta T_{t,L}\right) \qquad \textbf{Equation 2.1}$$

where φ is a calibration constant that accounts for the tip-sample contact resistance and resistance through the water meniscus and can be found through proper calibration against a known temperature standard. Figure 2.4 shows the results of this method, where subtraction of the non-contact signal in (b) from the contact signal in (a) reveals a highly resolved thermal image of the heated graphene channel.

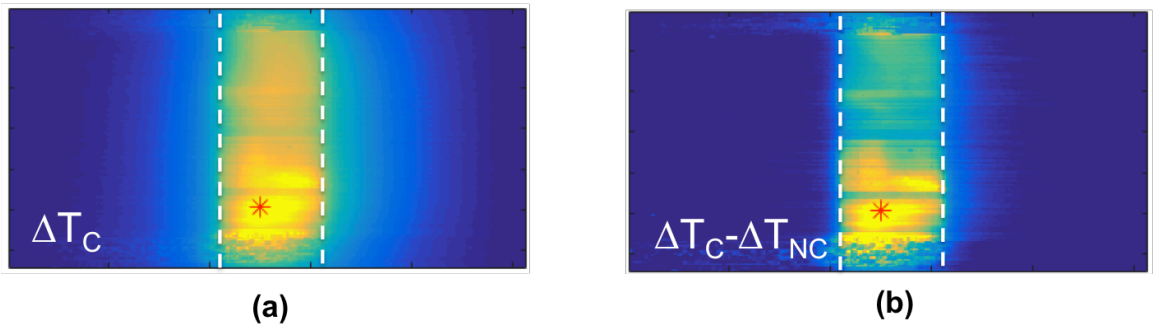

Figure 2.4: Thermal maps of a joule-heated graphene channel (outlined in white dashed lines) when the tip is (a) in contact with the sample and (b) when the lift mode profile is subtracted from the contact mode profile.

2.2.2 Electrostatic Force Microscopy (EFM)

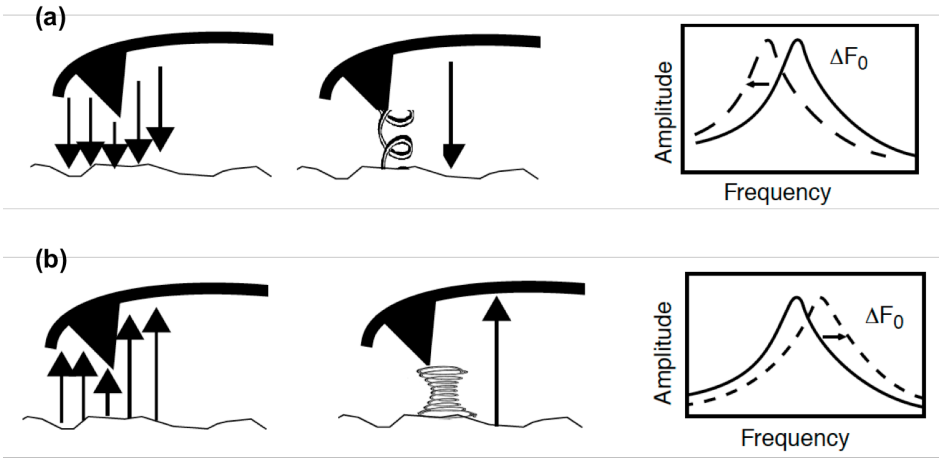

Figure 2.5: Working principles of EFM. (a) An attractive force between the tip and the sample is analogous to a spring in tension between the two, which causes a downshift in the resonant frequency of the tip in the tapping mode (i.e. an effective "softening" of the cantilever).[51] (b) A repulsive froce is analogous to a spring in compression connecting the sample and tip, which causes an effective "stiffening" of the cantilever and an accompanying upshift in the resonant frequency.[51]

Electrostatic force microscopy is another modified AFM technique, which allows direct visualization of electric potential gradients in an electrically biased sample. In this method, an electric potential is applied to an electrically conducting tip. Similar to SThM, EFM is conducted in two scans, one with the tip in contact with the sample and another with the tip lifted to a set height above it. In the lifted configuration, the long-range electrostatic force exerted on the tip by the electric field generated between the tip and the sample at different potentials causes a shift in the resonant frequency of the vibrating tip. An attractive force between the tip and the sample can be viewed qualitatively as a spring in tension connecting the tip and sample surface, as shown in Figure 2.5(a). Consequently, the tip behaves as if its cantilever has "softened," resulting in an observable downshift in the resonant frequency of the tip in tapping mode. The reverse is true for a repulsive electrostatic force between the tip and sample as shown in Figure 2.5(b). By tracking the shifts in resonant frequency as the tip scans, a qualitative image of the potential field of the sample can be visualized. In the following experiments, the particular EFM module that was used to track shifts in phase rather than frequency to produce the observed electric potential map, which is qualitatively similar to tracking shifts in the resonant frequency.

2.3 Experimental Setup and Device Fabrication

This section outlines the experimental EFM and SThM configurations used in this study. Details on the microfabrication process for the graphene electronic device are also given.

2.3.1 SThM and EFM Setup

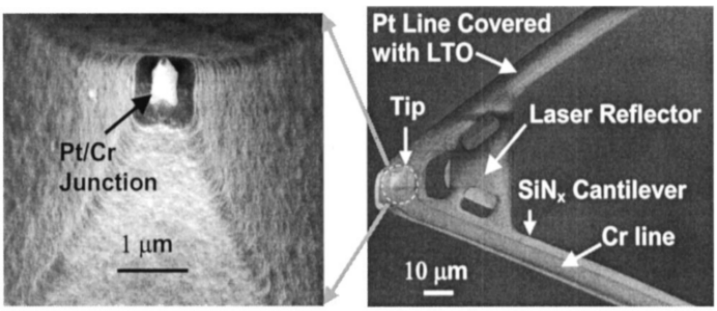

Figure 2.6: SEM image of a fabricated tip in the same batch as the one used in this study.[48]

For all experiments reported here, a Digital Instruments Multimode SPM with a Nanoscope IIIa controller was used in conjuction with a Signal Access Module, through which the relevant auxiliary electrical signal was collected (phase shift in EFM or thermoelectric voltage in SThM). A custom fabricated SThM probe with a V-shaped cantilever was used and consisted of a Pt-Cr thermocouple junction with a tip radius of approximately 20 nm as shown in Figure 2.6.[48] To maximize the thermal resistance of the probe, a low conductivity silicon nitride cantilever was designed to be 200 μm long with an 8 μm high SiO_2 tip. Due to thermally induced stress resulting from asymmetric metal deposition layers on the top and bottom surfaces of the cantilever, the soft SiN_x cantilever had a nominal 20° upward bend from root to tip. As shown in Figure 2.7, a custom tip holder was used to allow for electrical contact to be made to the junction. Furthermore, an aluminum wedge was filed to an appropriate angle to accommodate the upwardly bent tip and to maximize the reflected laser signal off the backside of the tip and into the photodetector in the AFM housing.

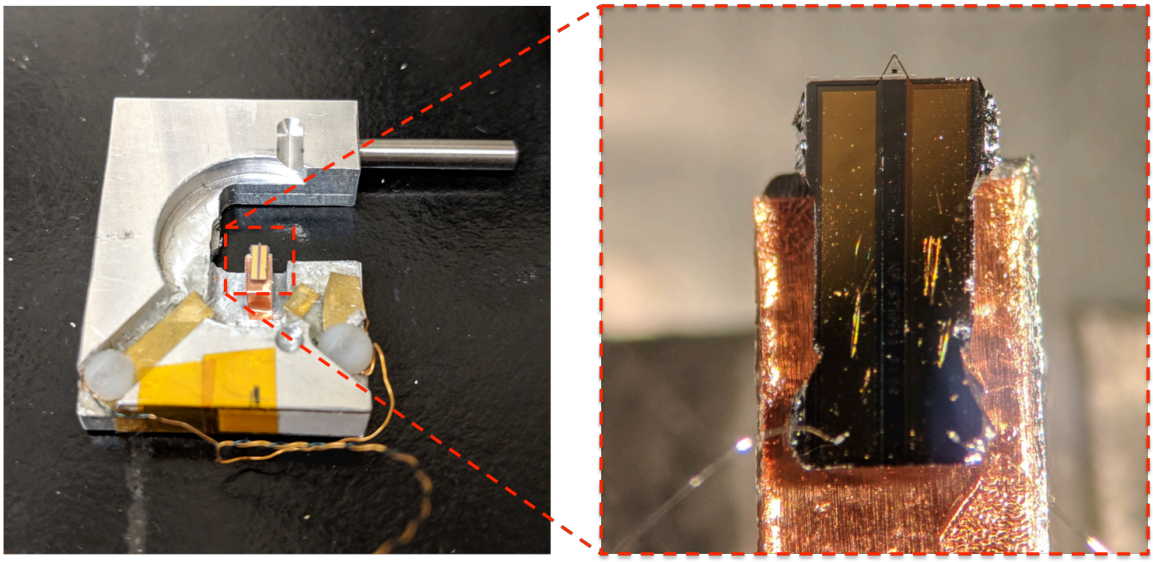

Figure 2.7: The custom AFM tip holder used in the experiments. The gold colored pads were connected to the bonding pads on the backside of the tip as shown in the enlarged section via wire bonding to establish electrical connection to the thermocouple junction.

2.3.2 Microfabrication of the Graphene Device

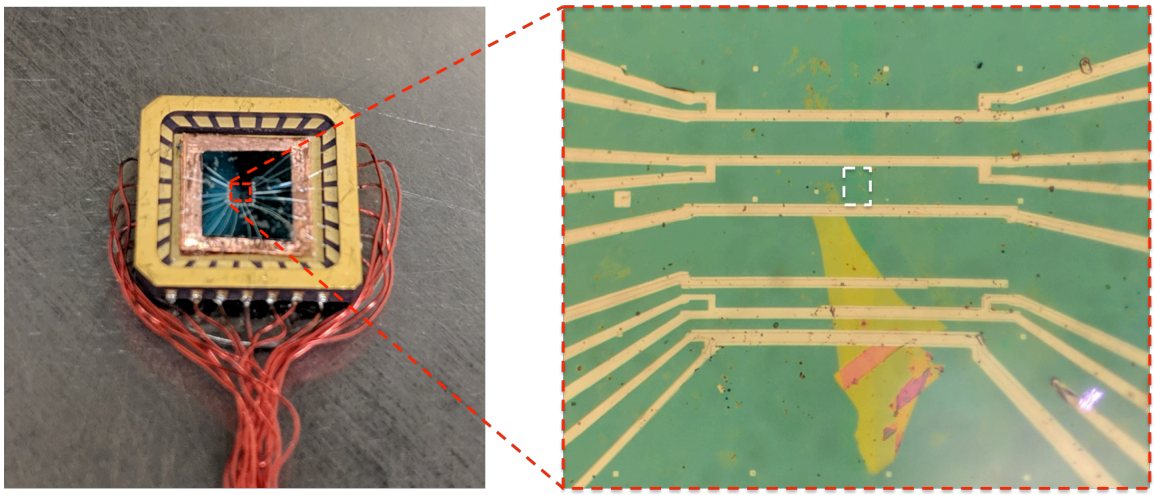

Figure 2.8: Optical image of the device mounted in and electrically connected to a chip carrier. The data in this section was obtained from the second graphene channel from the top, as outlined in the white dashed region in the enlarged view.

The graphene device used in this measurement was fabricated by Dr. Nirakar Poudel in Dr. Stephen B. Cronin's group at the University of Southern California. The sample consists of a 12.6 μm x 10 μm graphene channel on 300 nm thick SiO_2 on Si and is outlined in white-dashed lines in the exploded view. Low-pressure chemical vapor deposition (LPCVD) was used to grow the graphene at 1000 °C for 40 min on a copper foil for 40 minutes using a CH_4 feedstock. The large area graphene was transferred to the final substrate using a sacrificial polymethylmethacrylate (PMMA) transfer layer. After stripping the transfer PMMA, a fresh layer of PMMA is spun on the sample and the graphene channel was defined by electron-beam lithography (EBL). With the PMMA acting as a mask, the graphene channel was defined by oxygen plasma. A final EBL step to define the electrical contacts to the channel was followed by evaporation of 5 nm of Cr and 50 nm of Pd. The final device was annealed for 5 hours at 500 °C in an inert argon ambient to decrease the PMMA residue left on the graphene. The chip was then glued to a ceramic chip carrier using conducting silver paste and electrical connections from the carrier to device bonding pads were made using a wire-bonder. A more detailed account of this process is outlined in section 3.2.

2.3.3 SThM Calibration using the Double Scan Method

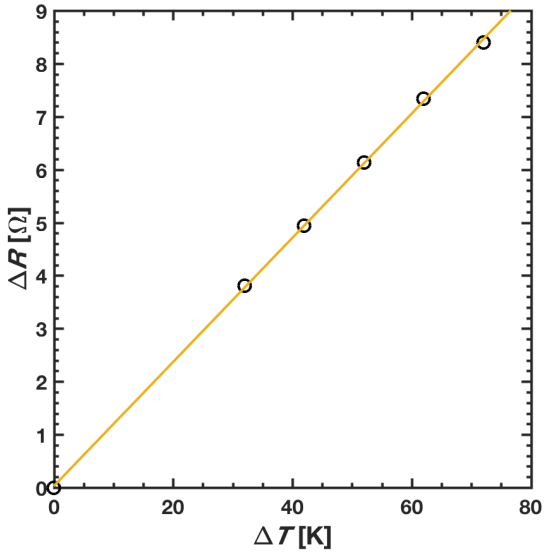

Figure 2.9: Change in four-probe resistance of the thermometer line as a function of the temperature rise from ambient in a box furnace.

The SThM tip used for obtaining the results reported in the manuscript was calibrated on a 100 μm long Cr/Pd thermometer line supported on 300 nm of SiO_2 on Si. In order for the thermometer line to act as a thermal standard against which the tip is calibrated, a relationship between the applied electrical current in the line and temperature rise due to joule-heating must first be established. The 4-probe resistance of the resistance thermometer device (RTD) was first measured as a function of temperature in a box furnace. The measured change in electrical resistance as a function of temperature rise is shown in Figure 2.9. The temperature coefficient of resistance, defined as $TCR \equiv \frac{dR/dT}{R_o}$ where R_o is the room temperature resistance, was calculated from the curve to be TCR = 0.00224 K^{-1}. To determine the average temperature rise in the line at a given applied current, the resistance of the RTD is related to the measured four-probe

votlage (V) and current (I) as $R = V/I$. To reduce the uncertaity at a small I value, a third order polynomial is fit to I-V data of the RTD such that:

$$V = a_3 I^3 + a_2 I^2 + a_1 I_1 + a_o \qquad \textbf{Equation 2.2}$$

where V is the applied 4-probe voltage, I is the measured current, and a_3, a_2, a_1, and a_o are constants of the fit. The resistance of the line as a function of current is calculated as:

$$R = \frac{V - a_o}{I} = a_3 I^2 + a_2 I + a_1 \qquad \textbf{Equation 2.3}$$

where the residual offset of the voltage amplifier circuit, a_o, has been subtracted. It then follows that the change in resistance as a function of current is:

$$\Delta R = R(I) - R(I = 0) = a_3 I^2 + a_2 I \qquad \textbf{Equation 2.4}$$

The temperature rise of the line as a function of measured current can be calculated as:

$$\Delta T = \frac{a_3 I^2 + a_2 I}{R_o \cdot TCR} \qquad \textbf{Equation 2.5}$$

Figure 2.10(a-d) shows the results from this process. To check the validity of the curve fit according to Equation 2.2, Figure 2.10(c) shows results of calculating the local slope (i.e. $\frac{dV}{dI}$) of the data in Figure 2.10(a) as a function of I. Each local slope was calculated from the best linear fit of each respective current in (a) and its 4 nearest neighbor values. The first coefficient of the fit in Figure 2.10(c) is 3 times that of the first coefficient in Figure 2.10(b), which correctly follows the mathematical descriptions of Equation 2.2 and Equation 2.3 thereby verifying the quality of the curve fit in Figure 2.10(a). Finally, Figure 2.10(d) shows the temperature rise as a function of I for the measured value of ΔT using the directly measured four-probe resistance of the line and

RTD and compares it to the ΔT predicted by the curve fits and Equation 2.5. Good agreement is seen between the two for a current value larger than about 2 mA, below which the directly measured four-probe resistance contains large uncertainty because of dividing the measured voltage with a vanishing current.

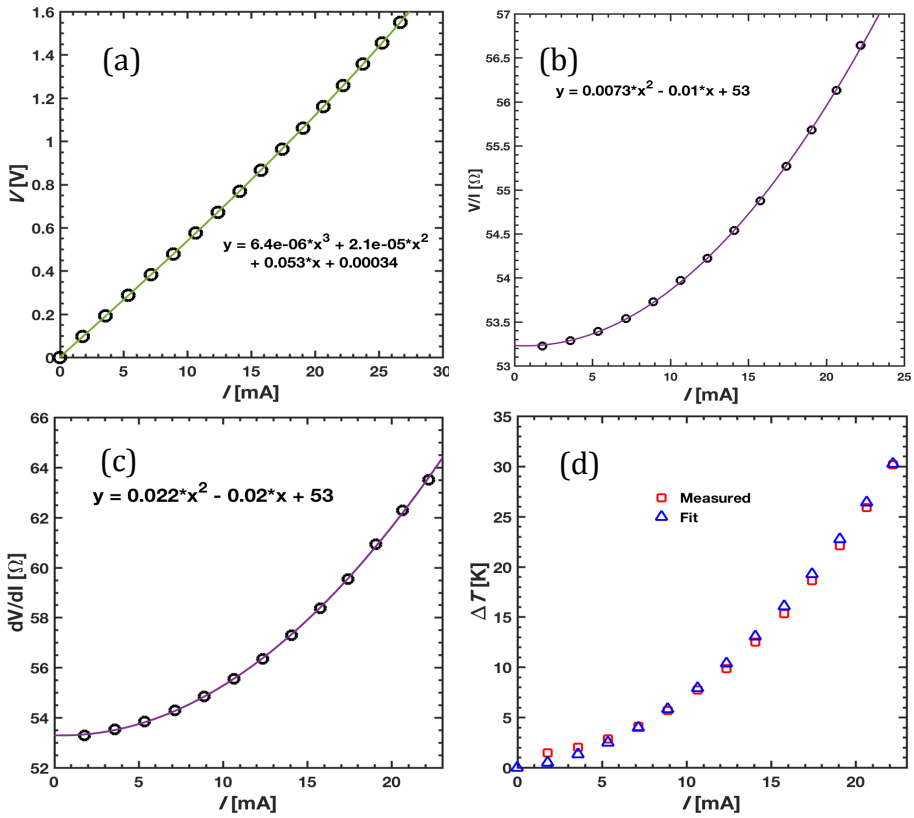

Figure 2.10: (a) Measured applied four-probe voltage as a function of measured current. (b) *V/I* as a function of current. (c) *dV/dI* as a function of current. Each local slope was calculated from the best linear fit of each respective current and its 4 nearest neighbor values. (d) Measured temperature rise as a function of measured current compared with the temperature rise predicted by Equation 2.5 and the data in (a).

Next the tip was calibrated against the RTD sensor at a known average temperature. Implicit in Equation 2.1 is that the thermopower of the thermocouple

junction is known. However, determination of S is typically destructive since the tip must be thermally equilibrated with a thermal standard, which requires fixation to a heater via an epoxy.[44] Because the variation in S within this custom fabricated batch was unknown, a slightly different calibration equation was used. Jo et al. reported a mathematically equivalent, yet experimentally simple implementation of Equation 2.1.[39] Assuming the thermovoltage in contact mode, ΔV_C, is linearly proportional to the sample temperature by a factor $\alpha < 1$, Equation 2.1 can be re-written as:

$$\Delta T_S = \frac{\varphi S}{1-\alpha}(\Delta V_C - \Delta V_L) = \beta(\Delta V_C - \Delta V_L) \qquad \textbf{Equation 2.6}$$

where β is a constant that can be found through calibration without the requirement of a known S.

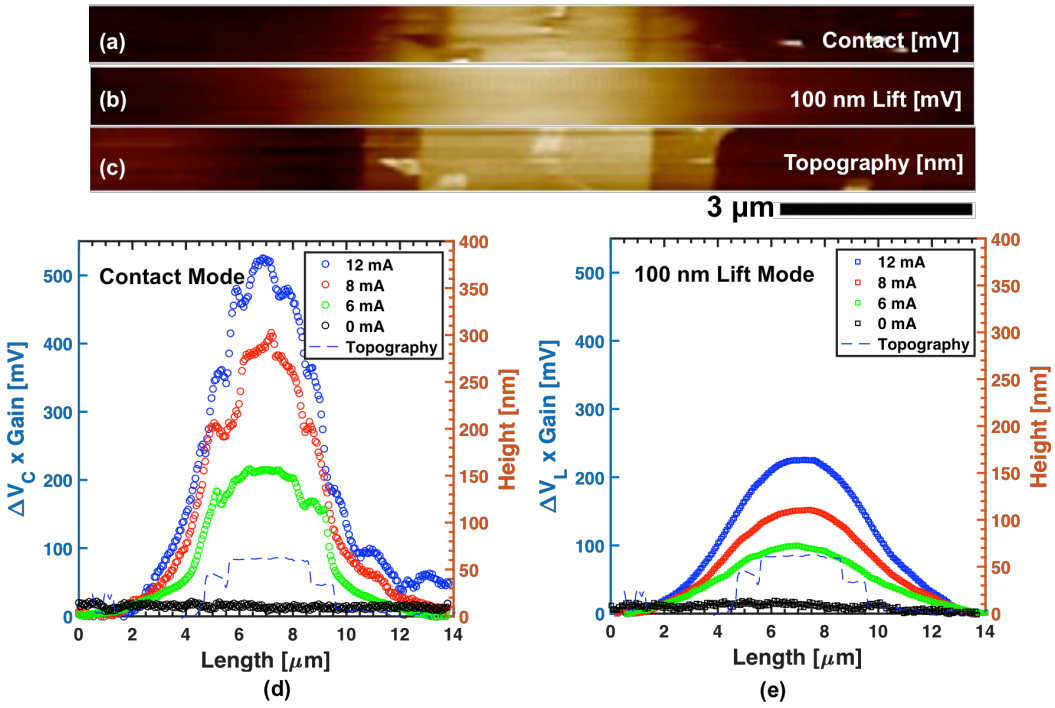

Figure 2.11: SThM calibration over a known thermal standard. (a) SThM scan over center of calibration standard line in contact mode. (b) SThM scan over center of calibration standard line at 100 nm lift height. (c) Topographical scan over center of

calibration standard line. (d) Line scans down the center of the contact mode scans at various heating currents. (e) Line scans down the center of the lift mode scans at various heating currents.

Figure 2.11 shows thermal and topographical scans over the center of the heated calibration line. The center of the line is supported by graphene and a 300 nm thick SiO_2 on top of highly thermally conductive Si. Owing to its small cross section and thermal conductance, the 5-μm wide monolayer graphene strip under the Pd line is not expected to significantly disturb the near uniform temperature profile of the thermometer line.[39] According to a numerical calculation, the center line temperature can be closely approximated by the average temperature of the line.[39] Figure 2.11(a-b) show the thermovoltage maps of the SThM scans when the tip is in contact with the line and when the tip is lifted to 100 nm above the line, respectively, while Figure 2.11(c) shows the topographical scan of the calibration line. Figure 2.11(d-e) are line scans down the center of (a) and (b), respectively, for various heating currents in the calibration line. Average values at the center point of each respective scan in Figure 2.11(a-b) were used to determine ΔV_C and ΔV_L. Finally, manipulation of Equation 2.6 allows for determination of the calibration factor β from a fit of the slope shown in Figure 2.12.

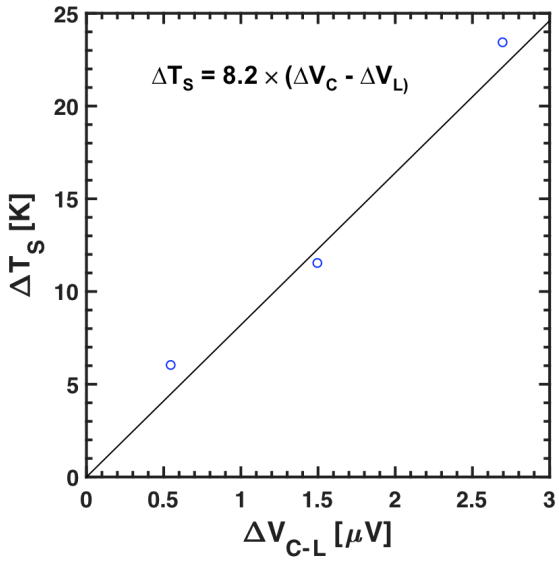

Figure 2.12: Determination of the calibration factor β by linear fit of Equation 2.6.

It is important to note that β could vary with different material surfaces. However, due to similar degrees of residual polymeric residue left on the device surface even after thorough cleaning, β has been shown previously to be insensitive to the surface material.[26,39,41,52,53] An in depth analysis using a similar tip to the one in this experiment is given in section 3.2.1.

2.4 Effect of Graphene Thermal Properties on Hot Spot Formation

The SThM and EFM experimental results of the joule-heated graphene channel shown in Figure 2.8 are discussed in this section. A thorough numerical and analytical discussion of the experimental results are used to describe the experimental findings and are extrapolated to reveal the relative importance of the graphene thermal conductivity and interface conductance on the magnitude of hot spots.

2.4.1 SThM and EFM Results of Graphene on SiO_2/Si

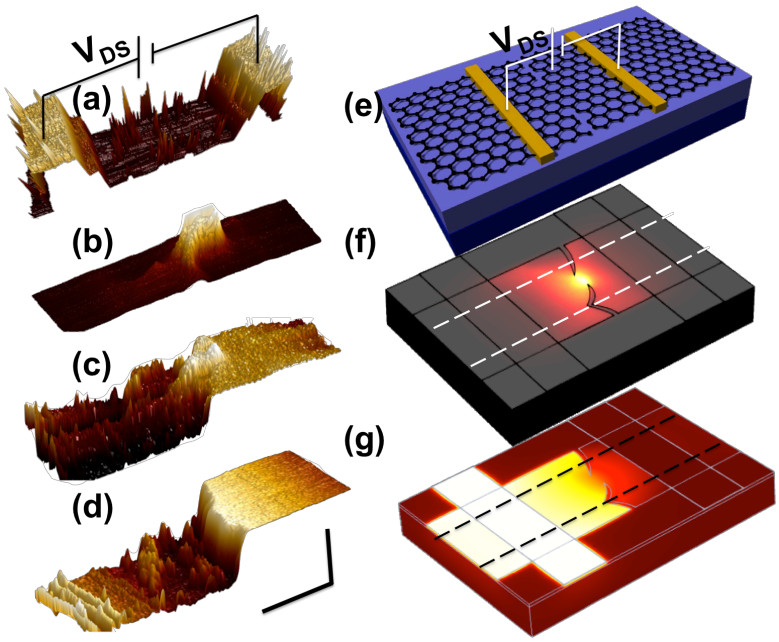

Figure 2.13: Measured [(a)–(d)] and calculated [(f) and (g)] topographic (a), thermal [(b) and (f)], and electrical potential profiles [(c), (d), and (g)] of the graphene channel, which are illustrated in a schematic (e). (a) Three- dimensional (3D) AFM image showing the topography of device. (b) SThM image showing a localized hot spot. (c) EFM image showing a steep potential drop at the location where the hot spot is shown by the SThM image. (d) EFM image after the constriction is destroyed by ESD, showing a step change in the surface potential that spans the entire channel signifying an open circuit. Horizontal scale bar is 5 μm and the vertical scale bar is 50 nm, 160 K, 4° and 10° phase shift for images a, b, c, and d, respectively. (e) Schematic of device. (f) Numerical calculation results of the temperature distribution around a constriction in the graphene channel. The two white dashed lines enclose the area shown in the SThM image in (b). The color scheme reflects temperature, with lighter colors indicating higher temperatures. (g) The corresponding calculated electric potential distribution, where the black dashed lines

enclose the area shown in the EFM image in (c). The color scheme reflects the electric potential, with lighter colors indicating a higher

Scanning thermal microscopy was used to quantify a large hot spot generated in the center of a 12.6 μm x 10 μm graphene channel supported on 300 nm SiO_2 on Si. Figure 2.13(a) shows the topographical scan of the channel, across which an electric potential was applied to the Cr/Pd electrical contacts. Figure 2.13(b) shows the measured temperature distribution on the graphene device when a 14 kW cm^{-2} dissipated power density was applied. For tear-free graphene devices measured in prior works,[39,54] the measured temperature profiles were smooth and diffuse within the channel, where a relatively large hot spot can exist because of non-uniformity in the local charge carrier density due to the variation in the gate electric field along the channel. Figure 2.13(b), in comparison, clearly shows a confined hot spot that is irregular in shape and concentrated in a very localized area. In addition, Figure 2.14 shows the experimental thermal profile through the center of the hot spot. The peak temperature rise was determined to be ΔT_{max} = 160 ±40 K, which is more than one order of magnitude larger than for a defect-free graphene channel with a similar power density dissipation.[39]

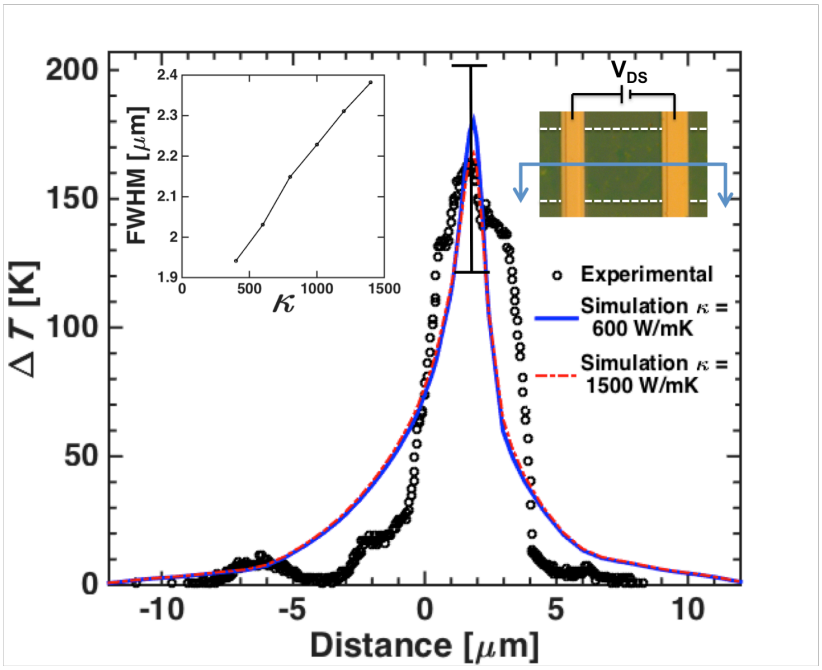

Figure 2.14: Comparison of experimental (symbols) and simulation results (lines) for the centerline temperature profile through the channel. Numerical results plotted for G = 9 × 10^7 W m^{-2} K^{-1}, κ = 600W m^{-1} K^{-1} (blue solid lines) and κ =1500 W m^{-1} K^{-1} (red dashed line). The left inset shows the increase of the full width at half maximum (FWHM) of the hot spot with increasing κ. The right inset shows an optical image of the channel under study on the device. The white dashed profile outlines the graphene channel, and the blue cross section indicates the location of the thermal profile shown in the figure.

To further examine the underlying cause of the observed hot spot in the graphene device, an EFM scan over the same channel was performed. The EFM probe (SCM-PIT, Bruker AFM Probes) consists of a Si tip on a Si cantilever. Electrical connectivity from the cantilever mount to the tip apex was established through a platinum-iridium coating. In a procedure similar to the non-contact SThM, EFM scans were performed in a lift mode to remove the topographical artifacts. An optimal lift height was determined by incrementally retracting the tip from the surface until the contact and lift scans showed a

minimal correlation. Figure 2.13(c) shows a sharp potential drop down the center region of the channel with discontinuous steps in potential on either side of a constriction. The steep gradient within the narrow strip of continuous graphene is coincident with and geometrically similar to the imaged hot spot, indicating the relation between the two. The SThM and EFM results suggest the presence of a defect tear in the graphene, which creates a micro-constriction in the channel. After the initial thermal and EFM scans were completed, the graphene channel was electrically broken by a large electrostatic discharge (ESD) current. Following this ESD, no current was observed upon application of a voltage bias to the channel. Figure 2.13(d) shows a potential discontinuity spanning the entire channel, confirming the breakage of graphene.

To better understand the experimental results, we have carried out a coupled electro-thermal transport simulation of the device. The geometry of the device, channel, and defect were reproduced in a numerical simulation through COMSOL Multiphysics with coupled electric and thermal transport equations. While the resistivity of electrically biased graphene has been shown to vary within the same channel, the resistance created by the experimentally observed narrow constriction is expected to be much larger than the variation due to the asymmetric distribution of charge carriers.[39] As such, an average graphene resistivity was specified to match the current resulting from the experimentally applied potential. Constant room temperature boundary conditions were specified on all lateral surfaces and the backside Si in the simulation domain. The thickness (t_{SiO2}) and thermal conductivity (κ_{ox}) of the SiO_2 film under the graphene were taken to be 300nm and 1.4 W m^{-1} K^{-1} , respectively. The thermal conductivity of the Cr/Pd line was calculated using the Wiedemann-Franz law and the measured four-probe electrical

resistivity of the line.[39] Using the basal-plane thermal conductivity and interface thermal conductance values of $\kappa = 600 \text{W m}^{-1} \text{K}^{-1}$ and of $G = 9.0 \times 10^{7}$ W m^{-2} K^{-1} reported in the literature for supported graphene,[35,55] the simulation predicts a $\Delta T_{max} = 180$ K, which is within the uncertainty of the experimental results. This calculated profile is plotted with the experimental data in Figure 2.14. The agreement suggests that the measured temperature rise can be explained with the literature κ and G values.

2.4.2 The Effects of Graphene κ and G on Reducing Device Operating Temperatures

Much attention has been devoted to developing fabrication processes and identifying suitable support materials to achieve graphene basal plane thermal conductivities near its theoretical limit via reduction of defect and substrate scattering of phonons. However, it is unclear whether the atomic thinness of graphene limits its ability to conduct heat in the basal plane such that interfacial thermal transport is dominant compared to lateral heat spreading.[25] It has been proposed that the interfacial thermal conductance between graphene and substrate could become the bottleneck in heat dissipation.[56] A detailed analysis to examine the impacts of these two thermal properties on the hot spot temperature on graphene electronic devices would be useful.

Therefore, an extended numerical study of the effect of thermal conductivity and interfacial thermal conductance was performed. The calculated maximum temperature rise is plotted as a function of κ in Figure 2.15(a) for increasing values of interfacial thermal conductance. Similarly, Figure 2.15(b) shows the predicted maximum temperature rise as a function of G for increasing values of κ. Several important conclusions can be drawn from Figure 2.15(a). The maximum hot spot temperature is

very sensitive to the thermal interface conductance when G is low, and insensitive when the conductance is high. For any given κ, the gradient $\frac{\partial T_{max}}{\partial G}|_{\kappa}$ is large for $G < 4 \times 10^7$ W m^{-2} K^{-1} and drops thereafter. For example, at κ = 600 W m^{-1} K^{-1}, increasing G from 1 × 10^7 to 2 × 10^7 W m^{-2} K^{-1} reduces the hot spot temperature by 40 K, whereas increasing G from 9 × 10^7 to 10 × 10^7 W m^{-2} K^{-1} only produces a 0.8 K reduction in maximum temperature. This behavior can be seen more clearly in Figure 2.15(b), where the effect of increasing G on ΔT_{max} quickly saturates, regardless of the graphene thermal conductivity.

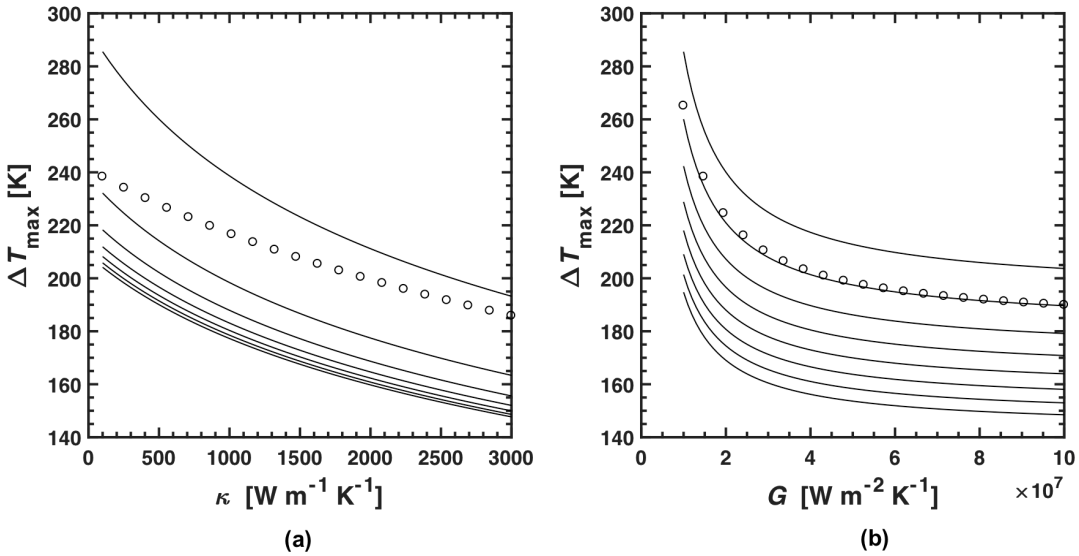

Figure 2.15: (a) The simulated maximum temperature rise as a function of the basal-plane thermal conductivity κ for different interfacial conductance G values in the range between 1 x 10^7 W m^{-2} K^{-1} (top curve) and 1 x 10^8 W m^{-2} K^{-1} (bottom curve) in increments of 1.5 x 10^7 W m^{-2} K^{-1} for the case of a 300- nm-thick dielectric. (b) The simulated maximum temperature rise as a function of increasing G for different κ in the range between 100 W m^{-1} K^{-1} (top curve) and 2900 Wm^{-1} K^{-1} in 400 W m^{-1} K^{-1}

increments. Representative curves calculated from the analytical solution of Equation 2.7 are pictured as open circles.

In contrast to the interfacial conductance, reductions in $\Delta T_{\max}$ do not saturate appreciably with increasing thermal conductivities. Within the range $300 < \kappa < 1200$ W m^{-1} K^{-1}, a maximum drop of ΔT_{max} from 565 K to 525 K can be attained for an interface conductance of 1×10^{7} W m^{-2} K^{-1}. Interestingly, increasing or decreasing G has relatively little effect on these results. For example, for the same range of κ, but with an order of magnitude larger interfacial conductance, a 20 K drop in ΔT_{max} is still observed.

These observed sensitivities of the maximum hot spot temperature to κ and G can be better understood with the use of the following simplified heat diffusion equation for the graphene channel in cylindrical coordinates, where the dependence on the azimuthal angle has been ignored:

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{dT}{dr}\right) - \frac{h}{\kappa t}(T - T_{\infty}) + \frac{\dot{q}'''}{\kappa} = 0 \qquad \textbf{Equation 2.7}$$

where r is the radial distance from the center of the hot spot, t = 0.335 nm is the thickness of graphene, $\dot{q}'''$ is volumetric heating in the unit of W m^{-3}, and h is the vertical heat transfer coefficient between graphene and the underlying silicon heat sink and is calculated as

$$h = \left(\frac{1}{G_{ox}} + \frac{1}{G}\right)^{-1} \qquad \textbf{Equation 2.8}$$

where $G_{ox} = \frac{\kappa_{ox}}{t_{ox}}$ is the vertical thermal conductance per unit area of the oxide layer. The volumetric heating term represents the joule heat concentrated around the defect and is approximated as a Gaussian distribution,

$$\dot{q}''' = \frac{q_o}{t} exp\left(-\frac{r^2}{r_o^2}\right) \qquad \textbf{Equation 2.9}$$

where r_o is a characteristic width of the localized heating spot. A value for r_o of 1.75 μm was obtained from the numerical simulation according to a fit of the J^2 profile, where J is the simulated current density. The constant q_o is obtained from the fit such that the total generated Joule heat is identical to that considered in the simulation. Equation 2.7 can be solved to obtain the temperature rise as a function of the non-dimensional term $z \equiv \frac{r}{l}$, where $l = \left(\frac{\kappa t}{h}\right)^{\frac{1}{2}}$ represents a heat spreading length, according to

$$\Delta T(z) = C_1 I_o(z) + C_2 K_o(z) + \Delta T_p(z) \qquad \textbf{Equation 2.10}$$

In this solution, I_o and K_o are the zeroth-order modified Bessel functions of the first and second kind, respectively.[35] The particular solution is of the form

$$\Delta T_p(z) = I_o(z) \int_0^z \frac{K_o(z) \frac{q_o t}{g} \exp\left(-\frac{z^2}{z_o^2}\right)}{-I_o(z)K_1(z) - K_o(z)I_1(z)} dz$$

$$-K_o(z) \int_0^z \frac{I_o(z) \frac{q_o t}{g} \exp\left(-\frac{z^2}{z_o^2}\right)}{-I_o(z)K_1(z) - K_o(z)I_1(z)} dz \qquad \textbf{Equation 2.11}$$

where $z_o \equiv \frac{r_o}{l}$. When subjected to the boundary conditions of a vanishing gradient at r = 0 and $\lim_{r\to\infty} T(r) = T_\infty$, $C_1 = -\lim_{z\to\infty}\left(\Delta T_p(z)/I_o(z)\right)$ and $C_2 = 0$.[35] Furthermore, the solution for the maximum temperature rise occurs at z = 0, where ΔT_p = 0 and I_o = 1. As such, $\Delta T_{max} = C_1$; which exhibits a similar dependence on G and κ as the numerical results, as shown by the open symbols in Figure 2.15**.**

This analytical model shows that $\Delta T_{\max}$ decreases with decreasing $q_0(1 + \frac{G_{ox}}{G})/G_{ox}$. Increasing G from 2 x 10^7 W m^{-2} K^{-1} to 2 x 10^8 W m^{-2} K^{-1} only results in a

small decrease of $\Delta T_{\max}$ for the case of a 300 nm SiO_2 where $G_{ox} \approx 4.7 \times 10^6$ W m^{-2} K^{-1}. This result arises because the G/G_{ox} ratio is larger than 4, such that the thermal resistance of the 300 nm oxide dominates the interface thermal resistance even for non-functionalized graphene with G as low as 2×10^{-7} W m^{-2} K^{-1}.[55,57] However, when the oxide thickness is reduced to 10 nm such that G_{ox} increases to about 1.4×10^8 W m^{-2} K^{-1}, increasing G from 2×10^7 W m^{-2} K^{-1} to 2×10^8 W m^{-2} K^{-1} via surface functionalization[58] or other means results in an increase of the G/G_{ox} ratio from about 0.14 to 1.4. This large increase helps to reduce $\Delta T_{\max}$ by nearly one order of magnitude, provided that the electron mobility of graphene is not reduced, and is shown in Figure 2.16**.**

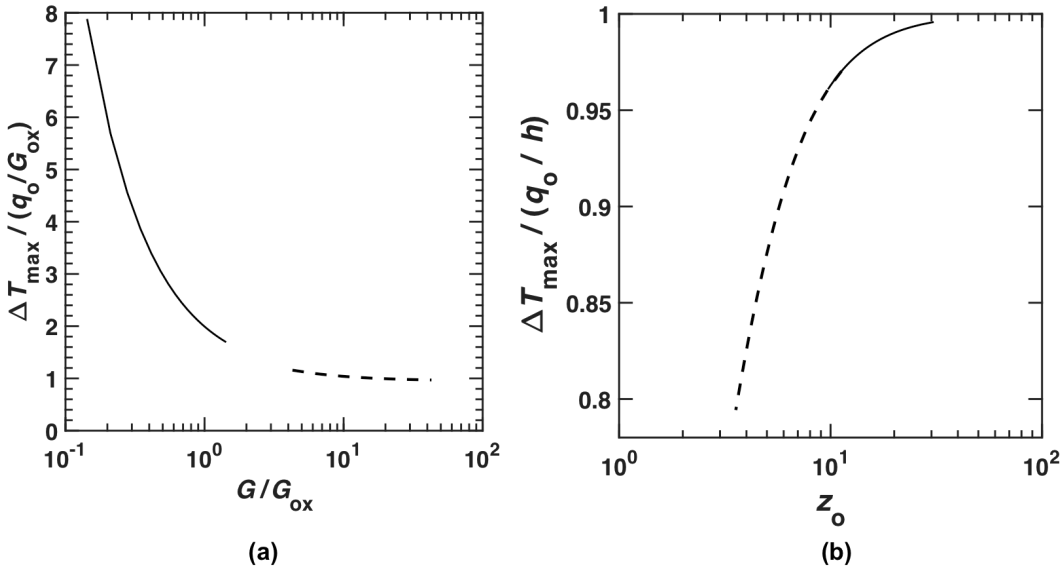

Figure 2.16: Normalized maximum temperature rise calculated by the analytical model as a function of (a) the *G/Gox* ratio and (b) the z_o parameter. The solid and dashed lines are for graphene devices made on a 10- and 300-nm-thick SiO2 dielectric on a high thermal conductivity substrate, respectively. The graphene basal-plane thermal conductivity is kept as 600 W m^{-1} K^{-1} in (a), and ranges between 300 and 3000 W m^{-1} K^{-1} in (b), where G is taken as 4×10^7 W m^{-2} K^{-1}.

In addition, the analytical model shows that $\Delta T_{\max}$ decreases with a decrease in $z_o = r_0/l$. When κ is increased from 300 W m^{-1} K^{-1} to 3000 W m^{-1} K^{-1} for the 300 nm thick SiO_2 device with a G value of about 4 x 10^7 W m^{-2} K^{-1},[55,57] the heat spreading length $l = (\kappa t/h)^{\frac{1}{2}}$ increases from 155 nm to 490 nm causing z_0 to decrease from 11 to 3.6. This increased l value is still smaller than the 6 μm lateral size of the graphene channel, so that the heat generated at the defect is not effectively spread to the metal electrodes. However, the l value becomes appreciable relative to the localized heat generation spot size r_0 of 1750 nm. The hot spot is therefore spread to a larger dimension laterally than r_0. Consequently, the effective area for vertical heat transfer from the hot spot through the oxide to the Si heat sink is increased, reducing $\Delta T_{\max}$ for the same localized heating profile. This result is shown in Figure 2.16(b). In contrast, when the oxide thickness is reduced to 10 nm, the heat spreading length is reduced to 57 nm and 179 nm for κ values of 300 to 3000 W m^{-1} K^{-1}, respectively. This length range is about one order of magnitude smaller than r_0 and corresponds to z_0 in the range between 30 and 9.8. As such, the relative increase in the hot spot area due to heat spreading is small. Increasing κ is therefore relatively ineffective for reducing $\Delta T_{\max}$ for the thin dielectric case, as illustrated in Figure 2.16(b).

2.5 Summary

This chapter used the SThM and EFM scanning probe techniques to identify and quantify the localized hot spot around a defect introduced in the transfer process of a CVD grown graphene channel onto an SiO_2/Si substrate. The numerical electro-thermal model is able to explain the measurement results based on reported thermal conductivity and thermal interface conductance values of supported graphene. The analytical model

further clarifies that increasing the thermal interface conductance G from the level of 4×10^7 W m^{-2} K^{-1}, as measured for non-functionalized graphene, is effective in reducing the hot spot temperature for devices made with a sub-10 nm gate dielectric on a high thermal conductivity substrate. However, when the cross-plane thermal conductance G_{ox} of the gate dielectric is not much higher than G, as is the case for devices made with a relatively thick gate dielectric or on a low-thermal conductivity polymeric substrate, increasing G via surface functionalization of graphene is ineffective. Furthermore, such functionalization can be counterproductive if the basal-plane thermal conductivity is reduced as a consequence of the functionalization process. In comparison, for a graphene device made on a 300 nm SiO_2 dielectric layer, increasing the graphene basal plane thermal conductivity from 300 W m^{-1} K^{-1} toward 3000 W m^{-1} K^{-1} can considerably increase the heat spreading length l compared to a micron-scale localized heat generation spot size, r_0, around a defect. This effect acts to increase the area for vertical heat transfer through the gate dielectric thereby reducing the peak temperature. This mechanism is effective even when lateral heat spreading from the hot spot to the metal electrodes is inefficient, i.e. when the lateral size of the graphene channel is much larger than l. However, the effect of increasing thermal conductivity becomes ineffective when l becomes considerably smaller than r_0, such as in a device made with a sub-10 nm gate dielectric on a high-thermal conductivity substrate. These results suggest that the hot spot temperature is sensitive to varying G and κ when the G/G_{ox} ratio and the r_0/l ratio are below about 5, respectively.

Chapter 3: Effect of an *h*-BN Heat Spreading Support on Hot Spot Temperatures in Silicon and Flexible Substrates[†]

3.1 Introduction

The revelation of the impressive electronic and thermal properties of graphene have motivated the exploration of not only this zero-band gap two-dimensional (2D) material but also other 2D semiconducting materials for next-generation electronic devices.[19–22,59,60] An emerging market for these 2D materials is in flexible and transparent electronics, where their high mechanical strength, optical clarity and electrical conductivity outperform those of many materials slated for use in similar roles.[22,26,30,61–64] However, most flexible substrates exhibit extremely low thermal conductivities on the order of 1 W m^{-1} K^{-1} as compared to their rigid counterparts, which is on the order of 150 W m^{-1} K^{-1} in the case of silicon. Therefore from a thermal perspective, devices fabricated on these substrates will behave significantly differently from those on silicon. Moreover, as the size of electronic components continues to shrink, the resultantly increased power densities generate localized hot spots that compromise the reliability and performance of the device. The low thermal conductivity and low glass-transition temperatures of most polymer or glass substrates mandate even stricter thermal management requirements on flexible platforms.[24,65] Compounding this issue of thermal dissipation, the large exposed surface area of 2D materials makes them susceptible to reduced electron mobility and

[†] The content of this chapter was published in D. Choi, N. Poudel, S. Park, D. Akinwande, S. B. Cronin, K. Watanabe, T. Taniguchi, Z. Yao, L. Shi, ACS Applied Materials and Interfaces, **10** (13), 11101 (2018). D.C. carried out the device fabrication, measurements, and analysis. N.P., S.P., S.B.C., and D.A. contributed to device fabrication. K.W. and T.T. synthesized the h-BN source materials. Z.Y. assisted in the scanning probe measurement. L.S. designed the experiment and contributed to the thermal measurements and data analysis.

thermal conductivity when they are supported on amorphous SiO_2 or polymeric substrates.[7–9] The reduced mobility leads to an increased power density at the same current, which cannot be dissipated effectively due to the reduced thermal conductivity. These issues have been found to result in high hot spot temperatures on graphene devices fabricated on both rigid and flexible substrates.[66,67]

Due to its atomic flatness, high-energy surface optical phonons, chemical inertness, and absence of dangling bonds, hexagonal boron nitride (*h*-BN) has recently been identified as a superior dielectric support for graphene and other 2D electronic materials. Besides enhancing the electron mobility of graphene, *h*-BN possesses a room-temperature in-plane thermal conductivity as high as 390 W m^{-1} K^{-1},[68] which is more than two orders of magnitude larger than most common dielectrics including SiO_2. In a previous study of self-heated graphene channels on a flexible polyimide substrate, Sadeghi and co-workers showed that despite the proposed benefit of graphene as a lateral heat spreader, heat transfer from the center of the device to the metal contacts for channel lengths longer than 1 μm is negligible since its atomic thickness limits its thermal conductance.[26] The high in-plane thermal conductivity of *h*-BN as a support for the active graphene channel may therefore increase the effect of lateral thermal spreading to a meaningful degree. However, since the cross-plane thermal conductivity of *h*-BN is only about 2 W m^{-1} K^{-1} and a significant amount of heat is dissipated vertically through the substrate, the thermal benefit of an h-BN support has not been assessed.[69]

The following study aims to address the outstanding questions and concerns regarding the efficacy of hexagonal boron nitride heat spreaders in conjunction with electronically active graphene channels. Quantitative scanning thermal microscopy is

used to study of the effect of an *h*-BN heat spreader for lowering the maximum temperature of micron sized hot spots in 2D electronic devices. The representative 2D devices used in this study are graphene channels fabricated on a 300 nm SiO_2/Si substrate and on a flexible Corning® Willow® Glass substrate.

3.2 Device Fabrication and Experimental Methods

This section outlines the device fabrication methods in detail. Furthermore, a more accurate method for calibration of the SThM tip than in section 2.3.3 is described. Finally, the triple-scan technique for SThM area mapping is explained.

3.2.1 *h*-BN Exfoliation, Graphene Growth, and Device Fabrication

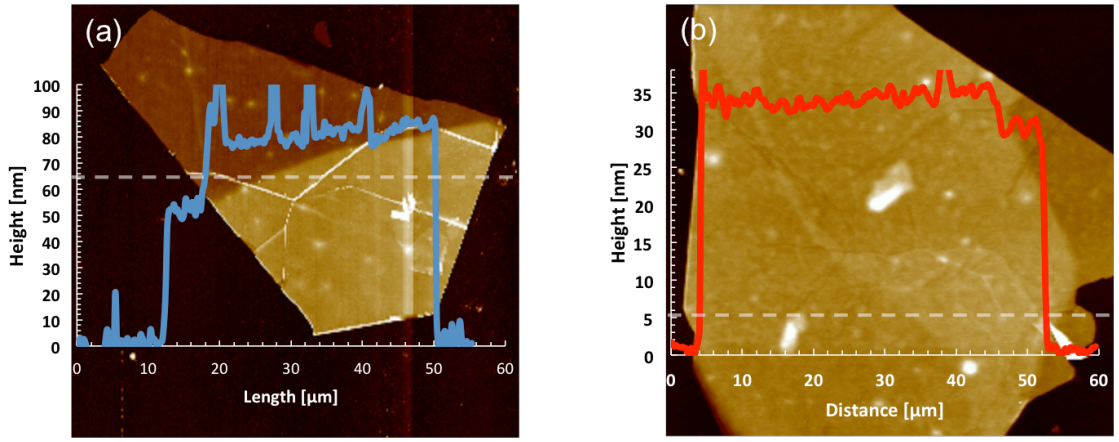

Figure 3.1: The *h*-BN flake thicknesses on (a) SiO_2/Si and (b) WG. The white dashed lines show the location of the respective AFM height profiles.

Hexagonal boron nitride flakes were exfoliated using Cleanroom Tape from high-purity hexagonal boron nitride (*h*-BN) powders onto either a 300 nm SiO_2/Si or Willow Glass® substrate. The *h*-BN powder was synthesized under high-temperature and high-pressure conditions using barium boron nitride as a solvent by our collaborators Kenji Watanabe and Takashi Taniguchi at the National Institute for Materials Science, Japan.[70]

The final thicknesses of the flakes were determined by AFM to be 80 nm and 35 nm on the SiO_2/Si and WG substrates, respectively, as shown in Figure 3.1.

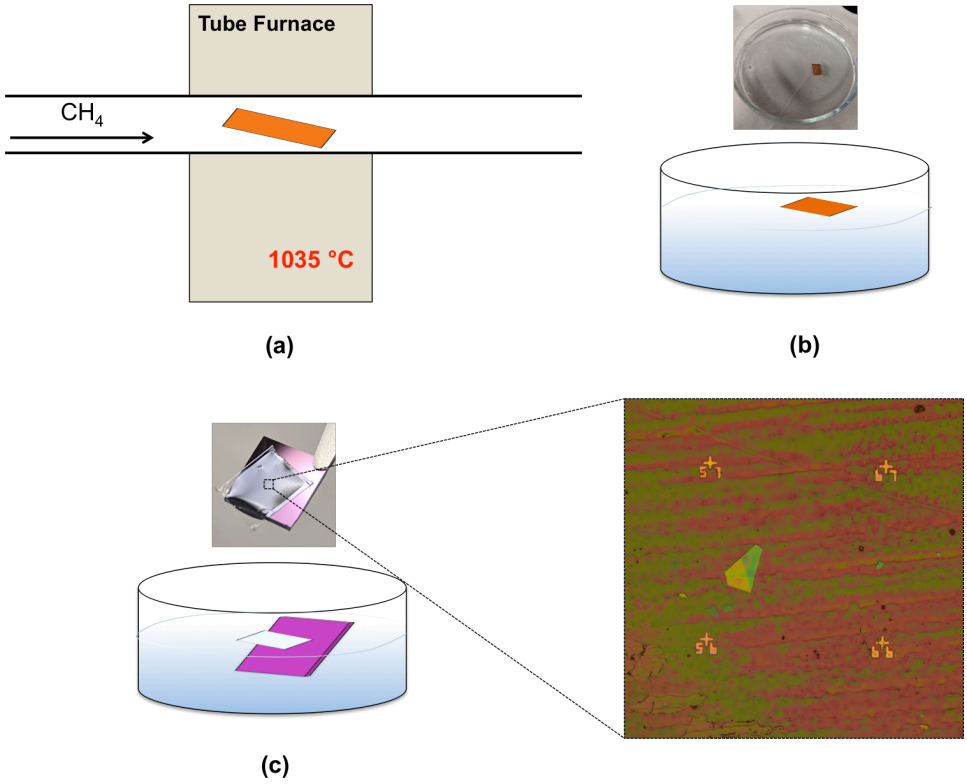

Figure 3.2: Graphene growth and transfer process. (a) A schematic of the copper foil in the tube furnace at 1035 °C under CH_4 flow. (b) After growth, removal of the backside graphene, and spin coat deposition of the PMMA transfer layer, the copper foil is floated on the surface of 0.15 M ammonium persulfate. (c) After dissolution of the copper, the floating PMMA layer is transferred to 3 separate water baths for rinsing. The transfer film is then scooped up using the final substrate where a suitable *h*-BN flake has already been exfoliated. The magnified optical image shows the same flake as in **Figure 3.1**(a).

The graphene samples used in this study were grown with low-pressure chemical vapor deposition (LPCVD) on a 25 μm thick copper foil (Alfa Aesar, 99.8% metal basis, stock number 13382). Before growth, the copper foil was pre-treated with a 2 hour soak

in undiluted acetic acid to remove the native oxide and surface copper layer followed by a 20 minute soak in HCl (10% by volume) and a quick deionized (DI) water rinse to remove the acetic acid. To smooth surface wrinkles and intrinsic curvature, the foil was sandwiched between two clean silicon wafer pieces and then inserted into a clean tube-furnace tube. The furnace temperature was ramped to 1000 °C in 30 minutes followed by a ramp to 1035 °C in 30 minutes under 5 sccm of H_2 flow. Once constant at 1035 °C, a 5 sccm flow of CH_4 was initiated to achieve a total pressure of 100 mTorr. After a 10 minute growth period, the furnace was manually turned off and the system was allowed to naturally cool to room temperature while maintaining both gas flows.

After growth, graphene is present on both sides of the copper foil. Since a PMMA assisted wet-transfer is used to transfer the graphene to the final substrate, the graphene on one side (the "backside") of the copper foil needs to be removed to allow for the eventual dissolution of the foil. A protective PMMA layer was first spun onto the front-side graphene at 3000 rpm for 1 minute and cured for 5 minutes on a hot plate set to 125 °C. The foil was then flipped so that the PMMA side faced down onto a glass slide and the periphery was taped. After fine-grit sandpaper was lightly rubbed on the backside, the sample was exposed to oxygen plasma to completely remove the unwanted graphene. The exposed copper was then floated face down on the surface of 0.15 M ammonium persulfate for 4 hours. After copper dissolution, a spoon was used to scoop and transfer the floating PMMA/graphene film to three subsequent water baths for rinsing. The final substrate (with *h*-BN exfoliated on the surface) was then used to scoop the PMMA/graphene film from the surface of the final water bath and set aside for an initial 30 minute drying period in air followed by a final drying process on a hot plate set

to 120 °C for 1 hour. After stripping the sacrificial PMMA transfer layer in 60 °C acetone for 2 hours, the sample was annealed at 350 °C in atmosphere to burn any remaining PMMA residue.

A rectangular graphene strip was then patterned by electron-beam lithography (EBL) and etched by an O_2 plasma at 100 mTorr and 50 W power. Electrodes were defined by a second EBL step and deposited by evaporation of 5 nm Cr and 50 nm Pd. After liftoff in 70 °C acetone, the final device was annealed at 350 °C in air for 10 minutes in an attempt to burn off residual PMMA. The final Joule-heated graphene channels under study measured 5 μm across and 10 μm long. Figure 3.3(a) and (b) show optical images of the final devices fabricated on 300 nm SiO_2/Si and Willow Glass, respectively. While optical contrast on the oxide allows for direct visualization of the channel (purple rectangular strip in Figure 3.3(a)), it is optically transparent on WG and is therefore outlined by the white dashed profile in (b) for clarity.

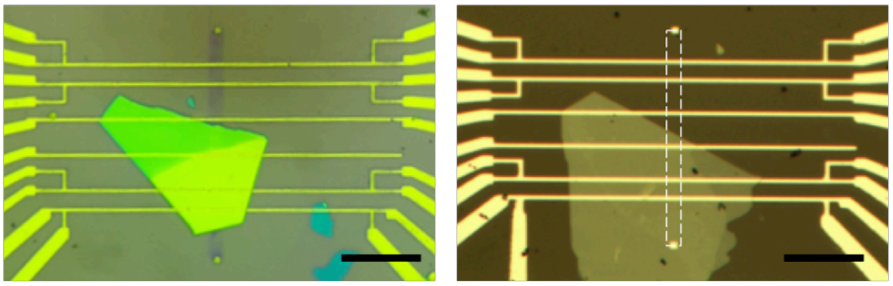

Figure 3.3: Optical images of the measured devices on the SiO_2/Si substrate (a) and the Corning® Willow® Glass substrate (b). The white dashed line in (b) shows the location of the full graphene strip. The scale bars are 25 μm.

3.2.1 SThM Calibration with the Force Curve Method

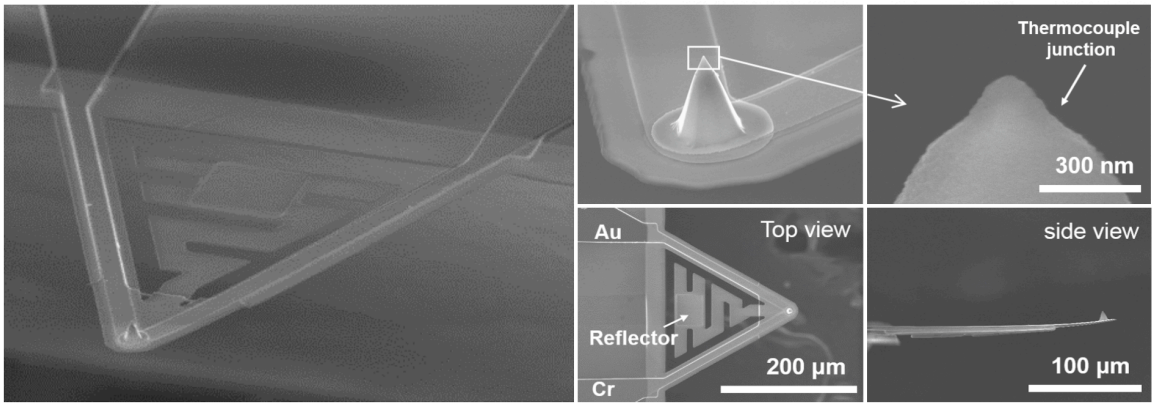

Figure 3.4: SEM image provided by TSP Nanoscopy of the NP SThM 02 tip used in the experiments of this section.[71]

The thermal probe used in the devices in these experiments was a commercially available SThM tip (NP SThM 02) purchased from TSP Nanoscopy and is shown in Figure 3.4. The specified 10 µm ± 1 µm high SiO_2 tip with a 70 ± 10 nm tip radius was attached to the probe body by a 200 µm long SiO_2 cantilever. The thermopower of the Cr/Au thermocouple junction was specified by the manufacturer to be 20.5 µV K^{-1}.

The φ parameter in Equation 2.1 was obtained from a calibration on a long Pd line acting as a resistance thermometer to calibrate the SThM probe. The thermal calibration standard was characterized in the same manner as that in section 2.3.3, where the measured four-probe current-voltage (*I-V*) curve of the Pd line was first used to calculate its electrical resistance increase due to Joule heating as a function of current. The resistance increase is then converted to the temperature rise with the use of the separately measured temperature coefficient of resistance (TCR) of the Pd line.

The double scan technique in section 2.3.3 described the tip calibration procedure assuming an idealization where the height of the lifted scan contained the exact same

thermal contribution through the air as when the tip was in contact with the sample. While this assumption is true for sufficiently small lift heights, there is in general a linear relationship between the temperature rise in the tip caused by heat transfer through the air and the lift height above the sample. Experimentally, however, maintaining stable lift heights of < 100 nm are difficult since the attractive van der Waals (vdW) and liquid meniscus forces between the tip and sample tend to pull the tip into contact with the surface. Intuitively, as the tip moves farther from the surface, the induced temperature rise in the thermocouple shrinks. Without taking this signal dependence on lift height into account, the calculated measured temperature is an overestimate of the true value. Consequently, the force curve method has been used in this calibration to eliminate this error by measuring ΔT_L (or ΔV_L) more accurately.[26]

In the force curve calibration method, contact and lift mode signals are obtained from a force curve of the tip onto the center of the RTD line, shown in Figure 3.5. As the tip approaches the surface, there is at first a linear increase in the thermovoltage from point A to point C while the tip is still not in contact with the surface. The tip jumps to contact from point C to point D due to vdW force and a thin liquid meniscus bridge that forms due to ambient moisture and is manifested by the sharp change in the deflection signal indicated in Figure 3.5(a). The jump to contact can also be observed in the thermal signal as a large jump in the thermovoltage shown in Figure 3.5(b). Furthermore, the vertical distance travelled by the tip between points C and D is only ~10 nm, which is closer to ideal than the 100 nm lift heights previously used. After contact, the thermal signal is not observed to change much with the applied contact force. This feature can be attributed to the dominant heat transfer through the liquid meniscus layer surrounding the

tip-sample contact.[26] Using the specified S of the tip, $\Delta T_{t,C}$ and $\Delta T_{t,L}$ in Equation 2.1 were determined by the thermovoltage signals at points D and C in Figure 3.5(b), respectively.

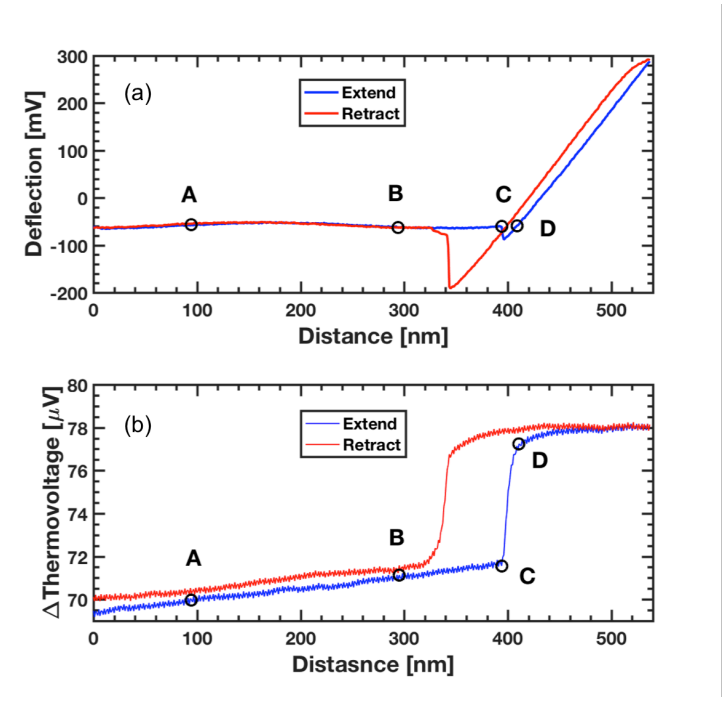

Figure 3.5: (a) Example force curve used for calibrating the tip. The tip is lifted to 300 nm and 100 nm above the sample at points A and B, respectively, and jumps to contact right after point C. Point D is where the contact mode thermal profiles were conducted. (b) Change in the thermovoltage signal as a function of distance from the surface. The thermal signal varies approximately linearly with the tip-sample gap distance between points A and C before the tip contacts the sample, and does not exhibit large changes with the contact force at point D and beyond after the tip makes contact to the sample.

Figure 3.6 shows the determination of φ by a linear regression fit at different currents through the RTD, where the fit satisfies:

$$\varphi_{fit} = \frac{N\sum_{i=1}^{N} X_i Y_i - \sum_{i=1}^{N} X_i \sum_{i=1}^{N} Y_i}{N\sum_{i=1}^{N} (X_i)^2 - \left(\sum_{i=1}^{N} X_i\right)^2} \qquad \textbf{Equation 3.1}$$

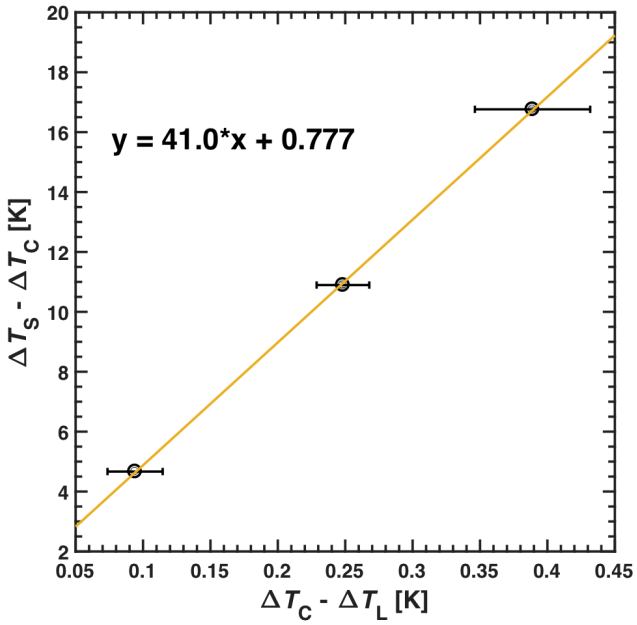

Figure 3.6: Determination of φ by linear fit at different applied currents.

The horizontal and vertical uncertainties, P_{X_i} and P_{Y_i}, respectively, in each data point in Figure 3.6 were determined from $P_i = t_{95}\sigma_i$, where t_{95} is the t-distribution and σ_i is the standard deviation of the set of Y_i or X_i data points.

Since φ is a measure of the thermal resistance between the sample and the tip, it is necessary to investigate the validity of using a single φ value for all regions of the scan where the tip moves from contact with SiO_2 or WG to graphene, *h*-BN or the metal electrical contacts. To study the effect of a changing surface, another tip with known *S* was used to evaluate the variation of the calibration constant (φ_{surf}) on different sample surfaces. In this experiment, the sample remained at room temperature such that $\Delta T_s = 0$. The thermocouple tip temperature rises, $\Delta T_{t,CL}$ and $\Delta T_{t,LL}$, due to laser heating were measured immediately after the tip made contact to the sample and after the tip was lifted

just out of contact from sample, respectively. The ΔT_s, ΔT_C and ΔT_L values were used in Equation 2.1 to obtain φ. The difference in the φ_{surf} values determined from this experiment on the Cr/Pd line, graphene/WG, graphene/SiO_2/Si, *h*-BN/graphene/WG, and *h*-BN/graphene/SiO_2/Si is smaller than the uncertainty in each obtained φ, as shown in Figure 3.7. The similar φ values are attributed to the presence of similar polymeric resist residue left on the different materials of the sample after the lithography process.[41,52] In comparison, the φ values of different tips can vary appreciably due to different tip radius values. The uncertainty in the final value of φ, $\delta_{\varphi,total}$, was calculated as a root sum square combination of the random uncertainty, $\delta_{\varphi,r}$ in the slope of Figure 3.6, and systematic uncertainty, $\delta_{\varphi,s}$ due to the variation in tip-surface interactions shown in Figure 3.7.

$$\frac{\delta_{\varphi,total}}{\varphi} = \sqrt{\left(\frac{\delta_{\varphi,r}}{\varphi_{fit}}\right)^2 + \left(\frac{\delta_{\varphi,s}}{\varphi_{surf}}\right)^2} \qquad \textbf{Equation 3.2}$$

where the uncertainty in the slope was calculated from the root sum square of the uncertainty propagated through the linear fit regression model:

$$\delta_{\varphi,r}^2 = \sum_{i=1}^{N}\left(\frac{\partial \varphi_{fit}}{\partial X_i}P_{X_i}\right)^2 + \sum_{i=1}^{N}\left(\frac{\partial \varphi_{fit}}{\partial Y_i}P_{Y_i}\right)^2 \qquad \textbf{Equation 3.3}$$

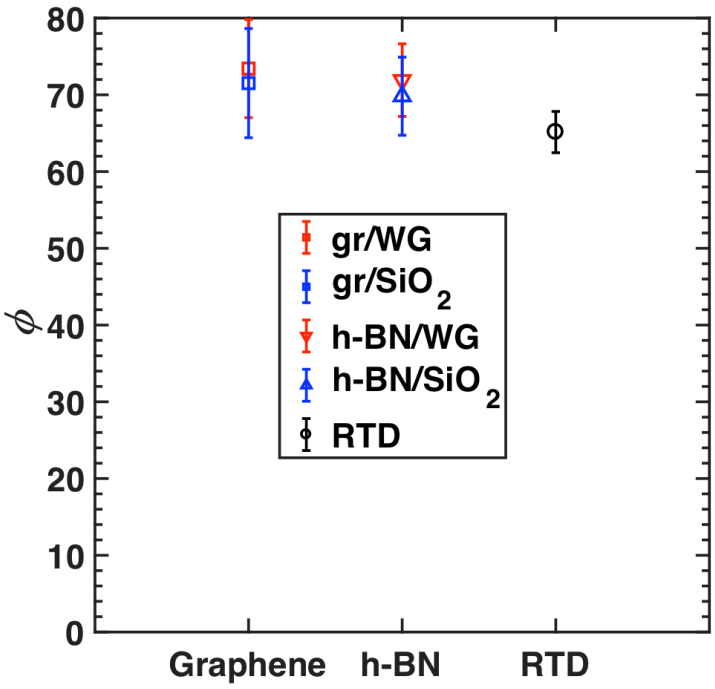

Figure 3.7: Measured φ values for tip contact with different sample surfaces.

3.2.2 The Triple Scan Method for Large Area SThM Mapping

In Figure 3.5 a force curve was used to determine the thermovoltage measured during the lift mode at near zero lift height, i.e. point C. During an actual area scan of the sample, however, obtaining a force curve for every point in the scanned area is time consuming and unrealistic. In order to obtain the thermovoltage at point C in Figure 3.5 for every point in the scanned area, a triple scan technique was used. Here, three scans of the same line are performed, once with the tip in contact with the sample and twice more with the tip lifted at different heights above the sample. In the experiments performed here, lift heights of 100 nm and 300 nm were used (points A and B in Figure 3.5) to extrapolate the lift signal to point *C*, which was used in calculating $\Delta T_{t,L}$. In reality,

because the AFM system allows only one contact and one lift height per line scan, a contact mode scan of the same line was performed for each lifted scan for a total of 4 scans per line (2 contact and 2 lift). An example of this process is shown in Figure 3.8. Figure 3.8(a) and (b) show the thermal map of the graphene channel on SiO_2/Si at 16 kW/cm^2 in contact mode and at 300 nm lift, respectively, with the hottest spots in each figure marked by a red "*". Figure 3.8(c) shows the subtracted temperature map. Figure 3.8(d) shows the two contact mode temperature profiles through the hot spot in Figure 3.8(a). Both contact line scans are nearly identical to one another. Figure 3.8(e) shows the thermal profiles through the hot spot in (b) when the tip is lifted to 100 nm and 300 nm as well as the calculated extrapolated curve to 0 nm lift height. Unlike the contact mode scans, there is a noticeable temperature difference between the two lift heights, analogous to that between points A and B in Figure 3.5(b). The sample temperature rise can be determined by subtracting the extrapolated lift temperature from the average contact temperature and plugging their values into Equation 2.1.

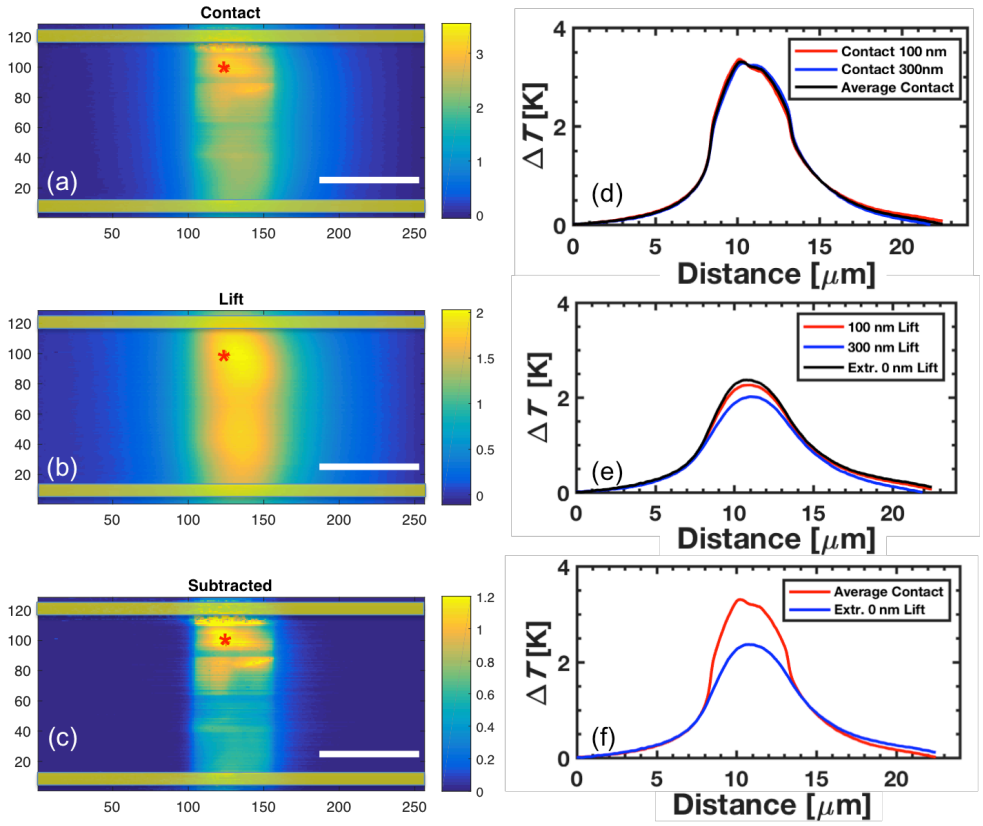

Figure 3.8: Thermal maps of graphene on SiO_2/Si at 16 kW cm^{-2} dissipation for (a) contact mode, (b) 300 nm lift mode, and (c) contact minus lift. Thermal line-scan profiles through the indicated hot spots in (a) and (b) are shown for (d) both contact mode scans along with their average value and for (e) 100 nm lift height, 300 nm lift height, and extrapolated zero lift height without contact. Figure (f) shows the average of the two contact mode profiles overlaid with the extrapolated lift mode profile. The scale bars in (a-c) are 5 μm. The color scale in (a)-(c) is in K.

3.3 The Effect of *h*-BN on the Thermal Profiles of Joule-Heated Graphene Channels on Silicon and Willow Glass

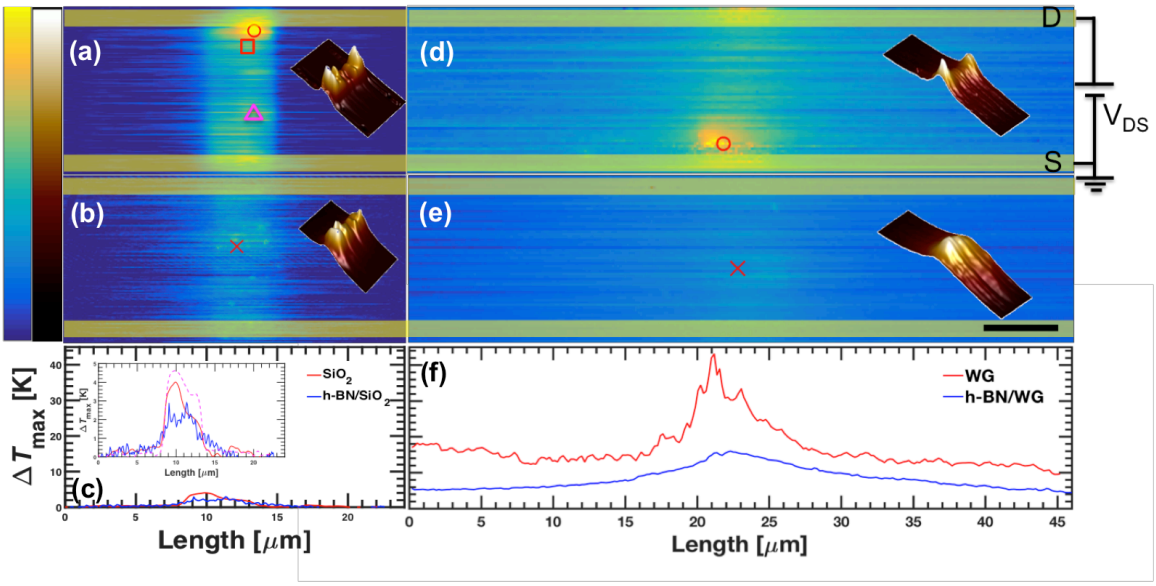

Figure 3.9: Thermal images of graphene supported on SiO_2/Si (a), *h*-BN/SiO_2/Si (b), WG (d), and *h*-BN/WG (e) substrates. The insets in the thermal images are three-dimensional temperature contours of the graphene channels. Each graphene channel was subjected to 2000 W cm^{-2} of Joule heating except for (d), where the power density is 1600 W cm^{-2}. The open circles "o" and "x" mark the locations of the hottest temperature in each image. The horizontal scan lines through each hot spot in (b), (d), and (e) are shown by the solid lines in figures (c) and (f). An expanded view of the main figure in (c) is shown in the inset for clarity. The open square in (a) is a different hot spot removed from the contact, whose horizontal scan line is plotted in the inset of (c) as the solid red line alongside a third scan line (dashed pink line) whose location toward the center of the channel is indicated by the pink triangle. The scale bar is 5 μm. The blue to yellow color bars range from 0 to 7 K for figures (a) and (b), and from 0 to 45 K for figures (d) and

(e). The black to white color bars for the 3D insets range from 0 to 3 K, 0 to 7 K, 5 to 20 K, and 10 to 45 K for (a), (b), (d) and (e), respectively.

SThM was employed in this work to study the effect of *h*-BN as a lateral heat-spreading layer between graphene and a 300 nm SiO_2/Si substrate as well as between graphene and a flexible Corning® Willow® Glass substrate, as shown in Figure 3.3(a) and (b), respectively. For the *h*-BN/SiO_2/Si sample shown in Figure 3.3(a), Joule heating was applied to the graphene section between the 4th and 5th electrodes from the top only, such that the underlying *h*-BN was of uniform thickness. Thermal scans performed perpendicular to the electrodes showed similar temperature profiles above the 4th electrode and below the 5th electrode, which can be attributed to a greater amount of heat flowing into the Pd electrode heat sinks rather than beyond them into other sections of the *h*-BN with variable thickness.

Figure 3.9(a–c) show the SThM results for graphene channels fabricated on an SiO_2/Si substrate. The images in Figure 3.9(a) and (b) are the thermal maps of graphene supported by SiO_2/Si and by *h*-BN/SiO_2/Si, respectively, and are plotted on the same 0 to 7 K scale. Both channels are subjected to a 2000 W cm^{-2} Joule-heat power density. The location of the maximum temperature in each section is indicated by the red "o" and "x". The yellow, horizontal bars indicate the location of the Cr/Pd electrodes and the insets show three-dimensional (3D) representations of each map. The temperature of a second spot several microns away from the contact and indicated by the red square in Figure 3.9(a) was chosen as the characteristic hot spot temperature for that device to avoid any possible effect of contact heating. Although it is difficult to see this hot spot at the 2 kW cm^{-2} power density, this spot was clearly visible in the SThM image obtained at the 16

kW cm^{-2} dissipation density, as shown in Figure 3.8(c) and indicated by a red "*" there. Figure 3.9(c) shows the thermal line scan through each respective characteristic hot spot indicated in Figure 3.9(a, b). An expanded view is shown in the inset for clarity, where a third scan through the spot indicated by a pink triangle in Figure 3.9(a) near the center of the channel has also been shown. Similarly, Figure 3.9(d) and (e) show the thermal images for graphene on WG under 1600 W cm^{-2} power density and graphene on *h*-BN/WG under 2000 W cm^{-2}, respectively. The temperature rise scale in these figures is 0 to 45 K. Figure 3.9(f) displays the line scans through the hot spots in these two devices. Figure 3.9(c) and (f) are plotted on the same scale to clearly illustrate the difference in thermal magnitude and distribution between the two substrates.

A comparison between the two different substrates reveals fundamental differences in both the magnitude of the temperature rise and the heat distribution. Figure 3.9(c) and (f) show that the maximum temperature rise of graphene on the thick, flexible WG substrate is an order of magnitude larger than that on the silicon substrate. For power densities of 1600 W cm^{-2} and 2000 W cm^{-2}, the maximum temperature rise of graphene on WG is 43.0 ± 6.1 K and the temperature rise at the characteristic hot spot on SiO_2/Si is 4.0 ±1.4 K. Similarly, the maximum temperature rises for graphene/*h*-BN/WG and graphene/*h*-BN/SiO_2/Si at 2000 W cm^{-2} are 16.0 ± 1.8 K and 2.9 ± 0.3 K, respectively. The much lower temperatures on silicon are attributed to the high thermal conductivity of the silicon substrate and relatively small thickness of the oxide layer compared to the channel width.[72] Consequently, heat is dissipated almost vertically through the SiO_2 and into the Si heat sink, as shown in Figure 3.9(a–c), where the temperature quickly drops to ambient within a couple microns laterally from the graphene

edge. In contrast, Figure 3.9(d–e) show elevated temperatures extending beyond 20 μm from the graphene edge on Willow Glass. Vertical heat transfer is therefore no longer dominant in the 100 μm thick WG, leading to a greater degree of lateral heat spreading and much hotter temperatures.

Because breakdown of graphene on bare WG was observed beyond the relatively low power density of 1600 W cm^{-2}, a direct comparison at an equal 2000 W cm^{-2} density for all devices was prohibitive. Moreover, the small temperature rise of graphene on *h*-BN/SiO_2/Si when dissipating less than 2000 W cm^{-2} was difficult to measure accurately. The study was therefore extended over multiple power densities to form a clearer picture of the heat transfer properties of both substrate types with and without inclusion of an *h*-BN layer. Figure 3.10 shows the hot spot temperatures increase linearly with increasing power density, and reveals that inclusion of an *h*-BN layer reduces the hottest spot temperature by a factor of about 2.2 and 4.1 for the devices fabricated on the silicon and WG substrates, respectively.

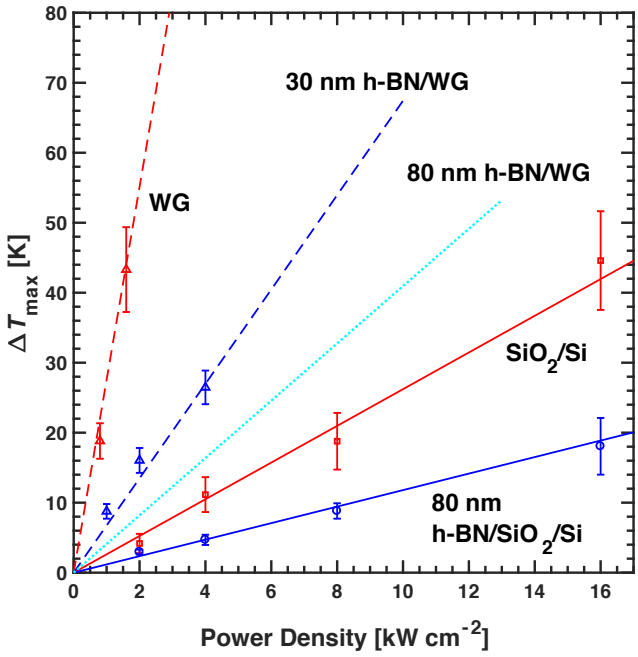

Figure 3.10: Maximum hot spot temperatures as a function of power density. The sky-blue dotted line indicates the analytical solution of a graphene device on *h*-BN/WG with the same 80 nm *h*-BN thickness as for the *h*-BN/SiO_2 case, while the analytical solution for the 35 nm *h*-BN thickness used in the actual sample is shown as the dark blue dashed line. Values of 2.8 μm, 4.0 μm, 4.0 μm and 5.3 μm for r_o, the characteristic hot spot radius, were used to fit the data for SiO_2/Si, *h*-BN/SiO_2/Si, WG and *h*-BN/WG, respectively and are comparable in magnitude to the experimental r_o values of 2.43 μm, 3.69 μm, 3.75 μm, and 7.8 μm, respectively.

It is necessary to discuss whether the observed reduction by the *h*-BN layer can be caused by the elimination of localized Joule heating, the heat spreading capability of the *h*-BN layer, or a combination of both factors. It is reported that an *h*-BN support can suppress electron-hole puddles[10,65] and change the Dirac point and carrier type in the graphene channel.[73] The four-probe resistance of the *h*-BN supported graphene channel

on SiO_2 was 3,320 Ω compared to the 970 Ω resistance of the graphene on bare SiO_2. Similarly, the four-probe resistance of the *h*-BN supported graphene channel on WG was 4,250 Ω compared to the 1,150 Ω resistance of the graphene on bare WG. The resistance increase with the *h*-BN layer is indicative of reduced electron-hole puddles and carrier concentration, as well as a shifting of the Dirac point toward 0 V. However, it is unclear whether electron-hole puddle suppression can potentially lead to increased uniformity of the Joule heat generation and thus reduced localized Joule heating.

The concentrated hot spots observed in the devices without the *h*-BN can in principle be caused by localized Joule heating due to contact heating, non-uniform charge carrier density, or non-uniform defect concentration along the graphene channel,[26,39,74–76] as well as Peltier cooling and heating at the contacts. Based on the measured two-probe and four-probe resistances of the graphene channel and the two-probe resistance of the electrical leads to the contacts, the contact resistance for the graphene/SiO_2 device of Figure 3.9(a) is only about 60 Ω, which is much smaller than the four-probe resistance of 970 Ω for the graphene channel and typical for such devices. Thus, the small contact resistance is not expected to be sufficient to generate the hottest spot near the drain contact for this device. However, to eliminate any ambiguity of the origin of the hot spot, only the temperature of the spot several microns away from the contact and indicated by the red square in Figure 3.9(a) is reported in Figure 3.10. For the graphene/WG device shown in Figure 3.9(d), the hottest spot centers at a distance of about 2 μm away from the actual contact, suggesting that the hot spot cannot be attributed to contact heating in this device.

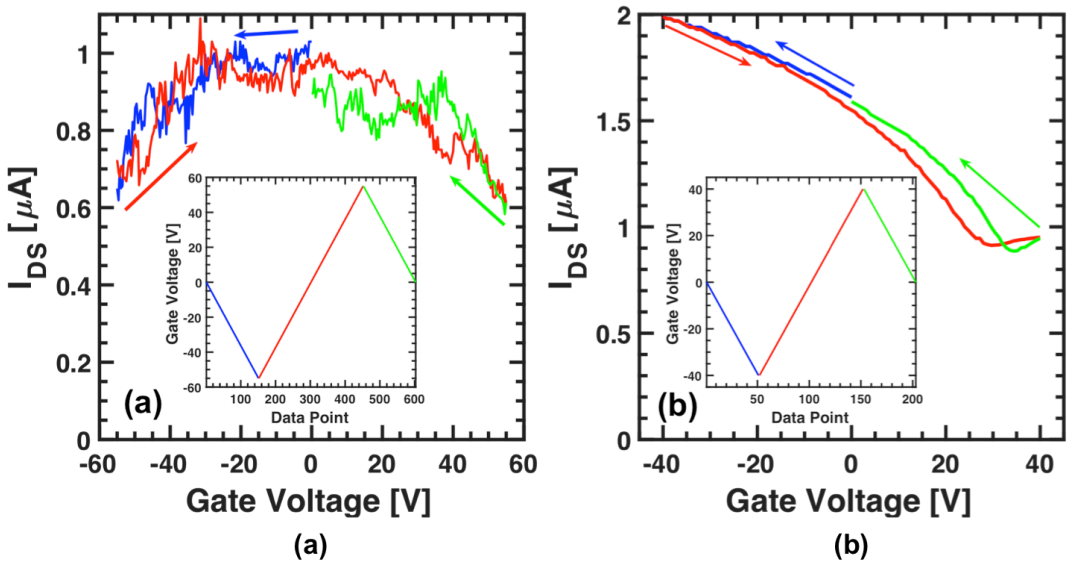

Figure 3.11: Two-probe gate-dependent measurements of the drain-source current (I_{DS}) at an applied drain-source voltage of 10 mV for the graphene channel supported by (a) SiO_2/Si and (b) h-BN/SiO_2/Si. The arrows show the direction of the voltage ramp for each colored section, while the insets show the overall gate voltage ramp scheme for each experiment.

In addition, the electron concentration of an *n*-type graphene channel is higher near the grounded source contact than near the drain contact where a positive drain-source voltage is applied, so that the resistivity and local Joule heating would be higher near the drain than near the source. The situation is reversed for a *p*-type graphene channel. Figure 3.11(b) shows the gate field-dependent current-voltage (*I*-*V*) measurements of the graphene channel on *h*-BN/SiO_2/Si and reveals that the channel is *p*-type. Despite being *p*-type, Figure 3.9(b) does not reveal the presence of a hot spot near the source electrode where the hole concentration is expected to be the lowest in this device. However, current leakage between a bonding pad and the silicon back gate through the 300 nm SiO_2 layer of the device without *h*-BN occurred after several ramping

cycles of the gate voltage and was visualized by a Schottky behavior in the IV curve. The gate leakage was therefore caused mainly by the damage of the thin oxide layer by a combination of a large mechanical force of the wire bonding tool and the large gate field. The leakage prevented determination of the majority carrier type of the graphene/SiO_2 channel, as shown in Figure 3.11. Hence, it is unclear whether the hottest spot found near the drain electrode for this device is caused by non-uniform carrier concentration, non-uniform defect concentration, or Peltier effect.

In spite of this uncertainty, it is apparent from the two thermal images in Figure 3.9(a) and (b) that most areas of the graphene channel without the *h*-BN layer are considerably hotter than the hottest point of the graphene channel with the *h*-BN layer at the same average power density. The dashed line in the inset of Figure 3.9(c) shows that the temperatures even at locations far away from the concentrated hottest spot in the graphene/SiO_2 device are in general higher than the hottest point in the *h*-BN supported channel. This comparison clearly suggests that the temperature reduction is mainly caused by the heat spreading effect of the *h*-BN layer instead of the presence of localized Joule dissipation only in the device without the *h*-BN layer but not in the device with the *h*-BN layer. A similar comparison can be made between the two devices on the WG substrate with and without the *h*-BN layer to reveal the heat spreading effect of the *h*-BN layer.

In order to better understand the main cause for the hot spot temperature reduction, an analytical model is established to gain physical insight into the heat spreading capability of the *h*-BN layer on the two different substrates. The cross-plane thermal conductivity of *h*-BN is in the range between 1.5 and 2.5 W m^{-1} K^{-1} at room

temperature. Thus, the cross plane thermal conductance of the *h*-BN layer is approximately 5×10^7 W m^{-2} K^{-1}, which is close to the interface thermal conductance between *h*-BN and graphene in a recent work.[69,77] In comparison, the cross-plane thermal conductance through the 300 nm SiO_2 is about 4×10^6 W m^{-2} K^{-1}, which is already much larger than the spreading thermal conductance of the 100 μm thick WG. Therefore, the temperature drop across the thickness of the graphene/*h*-BN stack is expected to be small compared to the temperature drops across the SiO_2 layer and the WG substrate. Consequently, both the graphene and the graphene/*h*-BN stack are assumed to act as a heat transfer fin with a uniform temperature across the thickness, such that the governing equation is:

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{dT}{dr}\right) - \frac{h}{\kappa_g t_g + \kappa_{h-BN} t_{h-BN}}(T - T_o) + \frac{\dot{q}''' t_g}{\kappa_g t_g + \kappa_{h-BN} t_{h-BN}} = 0 \qquad \textbf{Equation 3.4}$$

where T_o is the ambient temperature, h is the effective heat transfer coefficient between the ambient and the sample, t_g and κ_g are the thickness and in-plane thermal conductivity of the monolayer graphene, t_{h-BN} and κ_{h-BN} are the thickness and in-plane thermal conductivity of the *h*-BN layer, and $\dot{q}'''$ is the volumetric Joule heating in the graphene. The volumetric heating is assumed to take a Gaussian shape as that in Equation 2.9. Since Equation 3.4 is similar in form to Equation 2.7, it shares the same solution for the maximum temperature given as

$$\Delta T_{max} = -\lim_{z\to\infty}\left(\frac{\Delta T_p(z)}{I_o(z)}\right) \qquad \textbf{Equation 3.5}$$

where ΔT_p is given in Equation 2.11, where $z \equiv r/L_s$ and the heat spreading length L_s is given by

$$L_s \equiv \left(\frac{\kappa_g t_g + \kappa_{h-BN} t_{h-BN}}{h}\right)^{0.5} \quad \textbf{Equation 3.6}$$

The surface heat transfer coefficient, h, consists of a series combination of heat diffusion into the substrate and the interfacial thermal conductance between the sample and the substrate. Heat diffusion into the substrate is calculated differently for each case, and is reflective of the physical structure of the underlying support. With respect to the silicon substrate, vertical heat dissipation through the oxide is assumed based on the thermal scans shown in Figure 3.9(a –c). The surface heat transfer coefficient per unit area is therefore calculated as:

$$h_{SiO_2} = \left[\frac{t_{ox}}{\kappa_{ox}} + \frac{1}{G}\right]^{-1} \quad \textbf{Equation 3.7}$$

where t_{ox} is the SiO_2 thickness, κ_{ox} is the SiO_2 thermal conductivity, and G is the interface thermal conductance at the interface with SiO_2 per unit area. In contrast to the thin oxide layer, the isotropic, 100 μm thick WG substrate is much thicker than the width of the graphene channel. Therefore, the first term in Equation 3.7 is replaced with a three-dimensional thermal spreading resistance term for a circular hot spot above a semi-infinite medium, $R_{sp} = \frac{1}{4\kappa_{WG} r_o}$,[78] which is normalized by the area of the hot spot to yield:

$$h_{WG} = \left[\frac{\pi r_o}{4\kappa_{WG}} + \frac{1}{G}\right]^{-1} \quad \textbf{Equation 3.8}$$

where κ_{WG} is the WG thermal conductivity. In these models, a typical value of $G = 5 \times 10^7$ W m^{-2} K^{-1} reported in the literature was assumed.[79,80] Values for r_o of 2.8 μm, 4.0 μm, 4.0 μm and 5.3 μm were used to fit the data for SiO_2/Si, h-BN/SiO_2/Si, WG and h-BN/WG, respectively and are comparable in magnitude to the experimental r_o values of 2.43 μm, 3.69 μm, 3.75 μm, and 7.8 μm, respectively. The corresponding calculated values of ΔT_{max} are plotted in Figure 3.10 as dashed and solid lines and are in good

agreement with the experimental data. Equivalent to the effective hot spot thermal resistances per unit area, the slopes of these lines are 2.76×10^{-6}, 0.67×10^{-6}, 0.26×10^{-6}, and 0.12×10^{-6} m^2 K W^{-1} for WG, *h*-BN/WG, SiO_2/Si, and *h*-BN/SiO_2/Si, respectively.

According to these calculation results, the heat-spreading capability of the *h*-BN layer alone is able to yield a reduction in the hot spot temperature by a factor of 4.1 and 2.2 on the WG and SiO_2/Si substrates, respectively. Hence, the observed hot spot temperature reduction can be mainly attributed to the heat spreading effect of the *h*-BN layer, instead of the suppression of the localized Joule heating by the *h*-BN layer.

In addition, it is necessary to note that the experimental *h*-BN thickness on Willow Glass was 35 nm compared to 80 nm on SiO_2/Si. An additional analytical model for an 80 nm *h*-BN layer on WG is therefore included in Figure 3.10 as the dotted sky-blue line. The thermal resistance per unit area for this curve is 0.39×10^{-6} m^2 K W^{-1}, which predicts hot spot temperature reduction by a factor of 7.1 as compared to bare WG. The larger benefit of *h*-BN on WG compared to SiO_2/Si can be understood from the effect of the substrate-dependent heat transfer coefficient on the heat spreading lengths. Sadeghi and co-workers calculated that a large majority of the dissipated heat inside a graphene channel on a flexible substrate leaves vertically through the substrate itself rather than through the graphene toward the metal contacts.[26] As a result, it has been suggested that increasing the interface conductance, *G*, should be a key focus in improving thermal performance. However, for devices fabricated on a flexible substrate or a silicon substrate with an oxide layer thicker than ~100 nm where the substrate conductance is much smaller than the interface conductance, increasing *G* has a negligible effect on reducing hot spot temperatures.[81] In the experiments performed here, the first terms in Equation 3.7 and Equation 3.8, which represent the substrate through-

thickness thermal resistances, are both more than one order of magnitude greater than the second term, $1/G$, which is associated with thermal resistance of the interface. As a result, the analytical results found that even varying G to be as low as 1×10^7 W m^{-2} K^{-1} or as high as 10×10^7 W m^{-2} K^{-1} did not significantly affect the overall findings. Through-thickness dissipation is therefore dominated by the diffusive resistance of the substrate instead of the interface resistance.

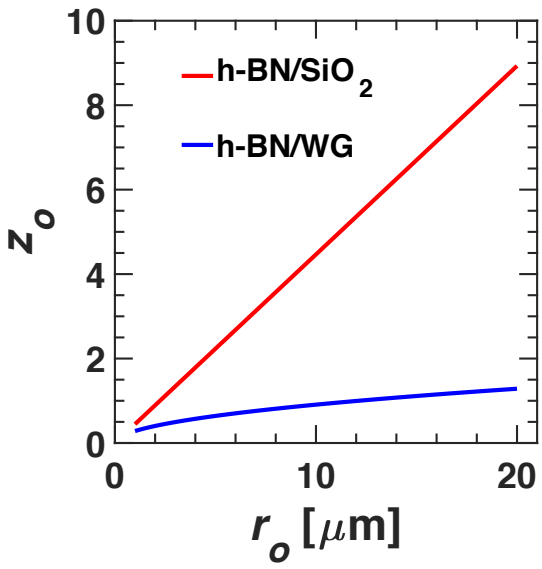

Figure 3.12: The dimensionless parameter z_o as a function of r_o for an assumed h-BN thickness of 50 nm.

Increasing the lateral footprint of the hot spot, however, can have a significant impact by enabling through-thickness dissipation over a larger area. In particular, increasing the heat spreading length relative to the hot spot size such that $z_o = r_o/L_s$ is less than about 5 is an effective method to reduce hot spot temperatures.[81] This approach remains effective as long as the heat spreading length is not much larger than the distance between adjacent hot spots, such that thermal cross talk is prevented. Figure 3.12 plots z_o as a function of the hot spot size for both substrates. This figure shows that inclusion of

an assumed 50 nm *h*-BN heat spreading layer can reduce the hot spot temperature effectively when the hot spot size on SiO_2/Si is less than 10 μm. Because of a lower h_{WG} value for 3D heat conduction through the WG layer compared to vertical heat conduction through the thin SiO_2 layer on the Si substrate, the z_o value is much lower for WG than for SiO_2/Si. Consequently, the z_o value for the *h*-BN/WG case is still close to 1 when the hot spot size is as large as 20 μm, such that the *h*-BN heat spreader is still expected to be effective if the separation between hot spots is larger than this length. The relatively large benefit of *h*-BN heat spreading on WG for larger hot spots follows naturally from Equation 3.8, where it can be seen that the heat transfer coefficient per unit area (h) decreases even further with increasing hot spot size on the WG substrate but not on the silicon substrate. As a result, the heat spreading length scales with the hot spot size on the WG substrate, but not on the SiO_2/Si substrate.

3.4 Summary

A force curve calibration method and triple scan technique were employed to perform quantitative scanning thermal microscopy of joule-heated graphene channels with and without an *h*-BN heat spreader on 300 nm SiO_2/Si and Willow Glass® substrates. The experimental and analytical results show that for equivalent power densities, inclusion of an *h*-BN layer between a graphene channel and its underlying substrate can result in a large drop in localized hot spot temperatures. Besides increasing the electron mobility, reducing electron-hole puddles, and shifting of the Dirac point, an *h*-BN dielectric layer below graphene serves as a highly effective lateral heat spreader and leads to a reduction of hot spot temperatures. The effective heat transfer coefficient per unit area is lower for three-dimensional heat conduction through a low-thermal

conductivity glass substrate than for one-dimensional vertical heat conduction through SiO_2 and decreases with the hot spot size for the WG substrate, but not for the SiO_2/Si substrate. As a result, the effect of the *h*-BN heat spreader is more pronounced for devices fabricated on a flexible glass substrate than on a SiO_2/silicon substrate due to a much larger heat spreading length. While localized heating inside individual 2D devices has been observed due to the presence of local defects or inhomogeneity in the charge carrier concentration, *h*-BN dielectric supports can reduce peak device temperatures by spreading hot spots laterally over the area between them.

Chapter 4: Thermal Conductivity Measurements of *h*-BN Encapsulated Graphene using a Suspended Microdevice

4.1 Introduction

Due to its very large surface area to volume ratio, many of graphene's attractive electronic and thermal properties are significantly reduced when it is brought into contact with a solid surface. For example, the thermal conductivity was shown to drop from 3000 W m^{-1} K^{-1} for suspended graphene to 600 W m^{-1} K^{-1} for oxide-supported graphene.[14,33] This provides the impetus for studies into the rational selection of a dielectric support.

Because of its small lattice mismatch with graphene, similar crystal structure, and the similar atomic masses of the B and N atoms compared to C, an *h*-BN support is expected to impart a different effect on phonon and electron scattering in graphene compared to an SiO_2 support.[82] For example, as compared to an SiO_2 support, the electron mobility of graphene on *h*-BN was seen to increase by nearly an order of magnitude[10] due to the reduction of electron-hole puddles and inhomogeneity in the charge carrier concentration.[7,83] The benefits of the closely matched lattice parameter also include an increased Seebeck coefficient and interfacial thermal conductance.[11,17,84] Similarly, a recent theoretical investigation has revealed that as compared to an 80% reduction of $\kappa_{graphene}$ on SiO_2 at room temperature, as little as 4% reduction is expected for *h*-BN supported graphene.[82] While the effect of the ZA mode suppression was similar to that on SiO_2, the calculation showed that this smaller reduction was due to a minimal effect of *h*-BN on the in-plane polarized vibrational modes.

In another theoretical study, Zhang and coworkers reiterated that the effect of the support was to suppress the low-frequency out-of-plane phonons more significantly than the intermediate and high-frequency in-plane modes.[16] The numerical results suggested that the *h*-BN substrate reduced the mean free path of the dominant heat-carrying phonon modes by only ~50% as compared to an ~88% reduction on SiO_2. A similar numerical prediction was put forth by Pak and Hwang who drew analogy to the support behaving as a high-pass phonon filter where the effective lower cutoff frequency varies depending on the substrate material.[18] Because the high thermal conductivity in suspended graphene is dominated by these out-of-plane low-frequency phonons, substrates like *h*-BN that impart a smaller effect on these modes should result in a larger thermal conductivity.[85]

Despite offering a rich set of physics to be explored and a suite of practical applications, no experimental data exploring the basal-plane thermal conductivity of *h*-BN supported graphene have been published to date. Therefore, in addition to significantly reducing hot spot temperatures as a passive heat-spreading layer as shown in Chapter 3, here we experimentally study the added benefit of an *h*-BN support on increasing the basal-plane thermal conductivity of graphene relative to an SiO_2 substrate.

Besides amorphous substrates, polymeric residues left on the graphene surface from microfabrication processes have shown to impart a similar scattering effect on phonons.[41,52,86] Several works have reported that even after thorough cleaning in heated solvents and annealing in various combinations of H_2, Ar, and air at temperatures up to 300 °C for several hours, TEM images show that a thin film of PMMA remains over a significantly large area of graphene.[41,52] In the study of interfacial phenomena then, it is imperative that a clean, polymer free interface is established between the *h*-BN and

graphene. A dry transfer method for stacking hexagonal boron nitride and graphene is used in this work such that the graphene sample was never directly exposed to any polymer during fabrication.[87,88] A detailed account of this process is outlined in Section 4.5.1.

Finally, while Raman spectroscopy has been used to determine the thermal conductivity of suspended graphene structures in the past, there remain concerns regarding its applicability and accuracy. For example, it was recently shown that the temperature of the measured optical phonons and the temperature of the heat-carrying acoustic phonons are driven out of thermal equilibrium within the small excitation beam spot size.[89] Conclusions about thermal transport properties using temperature distributions of phonons that are not at local equilibrium may therefore not be accurate. In contrast, temperature measurements in suspended microdevices using resistance thermometer detector sensors are relatively accurate and precise.[90,91] Therefore, a similar design and measurement scheme used by Seol and coworkers were adapted in this work to extract the thermal conductivity of *h*-BN encased graphene.[14]

4.2 Thermal Transport Measurements in Suspended Nanostructures

A thermal analysis of the suspended nanostructure is outlined in this section. First, the derivation of the relations between the experimentally measured temperature rises of the RTD sensors and the final graphene thermal conductivity is discussed. Next, a modification of the thermal design to improve the measurement sensitivity of the sample conductance is introduced. This analysis shows that for high conductance samples auxiliary support beams need to be added to the suspended structure to allow for efficient heat sinking to the substrate.

4.2.1 Thermal Analysis of Suspended Nanostructure

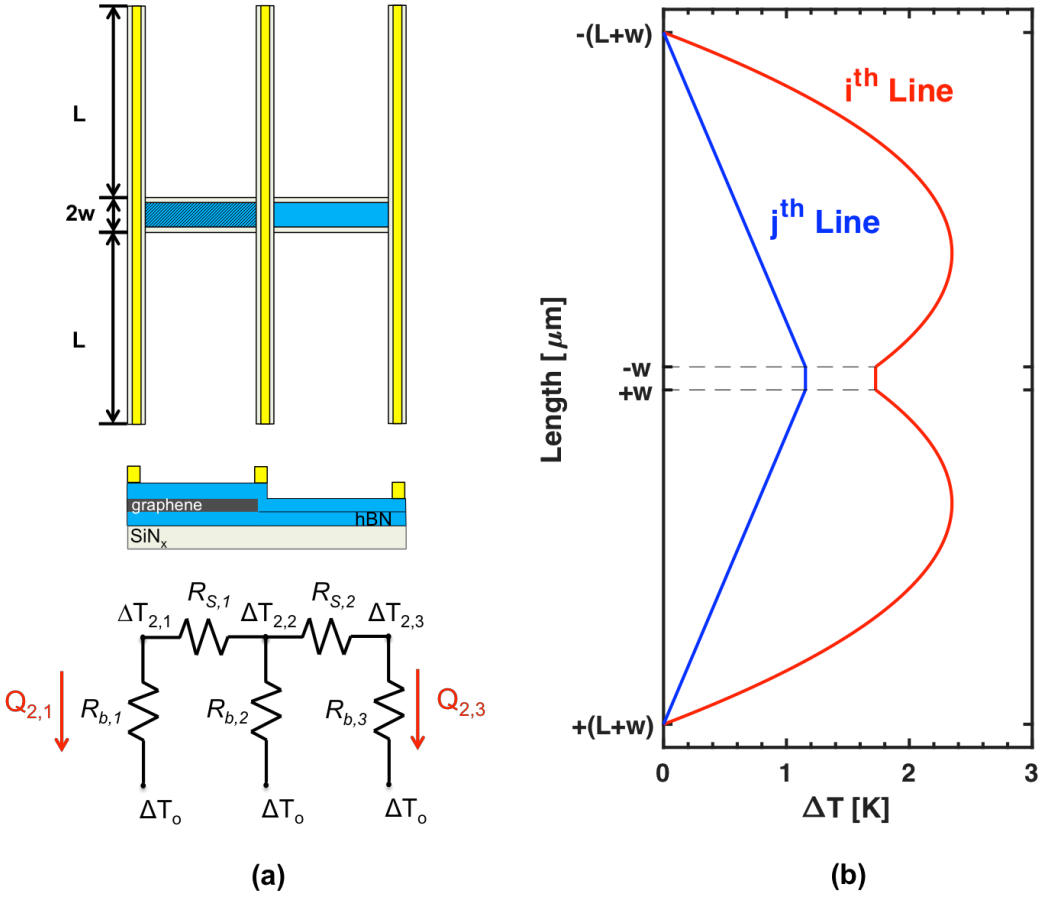

Figure 4.1: (a) Schematic of the thermal device with suspended measurement lines and sample sections. The equivalent thermal circuit is shown below the schematic, where the notation follows the case where line 2 acts as the heater line. (b) Thermal profiles as a function of the length along the heater (j^{th} line) and sensing (i^{th} line).

The thermal conductivity of graphene encapsulated by *h*-BN is determined using a suspended micro-device structure with two thermal sections. In the measurement, two continuous sections of the same sample are measured, one consisting of *h*-BN/graphene/*h*-BN/SiN_x ($R_{S,1}$) and the other *h*-BN/*h*-BN/SiN_x ($R_{S,2}$). When the thermal conductance of the relatively thick *h*-BN layers is assumed to be unaffected by the

graphene, the thermal conductivity of graphene encapsulated by *h*-BN is extracted from the difference in thermal conductance (inverse of resistance) between $G_{S,1}$ and $G_{S,2}$ and known graphene dimensions. A simple schematic of the device in this study is shown in Figure 4.1(a), which assumes line 2 acts the heater line. During the thermal measurement, one of the Cr/Au lines is joule heated (heating line denoted as *i = 1, 2,* or *3*), while the other two lines act as 4-probe resistance thermometers (sensing lines denoted as *j = 1, 2* or *3*, where $j \neq i$). For the heating line, a similar analysis as that in Section 2.3.3 can be used to relate the measured *I-V* curve to a measured average temperature rise of the line, $\overline{\Delta T_{i,J}}$. In contrast, the measured average temperature rise of the sensing lines, $\overline{\Delta T_{i,J}}$ is obtained directly from a 4-probe resistance measurement with a lock-in amplifier and the TCR of the line.

To solve the thermal circuit for the sample section resistances, we must first derive a set of equations to solve for the beam resistances, R_b, based on the experimentally measured average temperature rises of the lines, $\overline{\Delta T_{i,J}}$. Toward this goal, we first find the total heat flow through the sample sections, Q_{in}, by summing the heat flow through the sensing beams and out to the silicon substrate:

$$Q_{in} = \sum_{j,j\neq i} Q_{i,j} = \sum_{j,j\neq i} \frac{\Delta T_{i,j}}{R_{b,j}} \qquad \textbf{Equation 4.1}$$

where $R_{b,j} = \frac{L_j}{2\kappa_j A_j}$ is the total parallel thermal resistance of a given beam accounting for both sections on either side of the sample, κ_j and A_j are the thermal conductivity and cross-sectional area of the j^{th} sensing beam and $\Delta T_{i,j}$ are the temperature rise at the metal/sample contact. Equivalently, Q_{in} can be derived from the thermal profile in the heating line where:

$$Q_{in} = -\kappa_i A_i \left.\frac{d\Delta T_{i,x}(x)}{dx}\right|_{x=-w} + \kappa_i A_i \left.\frac{d\Delta T_{i,x}(x)}{dx}\right|_{x=w} + 2wA_i\dot{q}''' \qquad \textbf{Equation 4.2}$$

where $\dot{q}''' = \frac{(IV)_i}{2A_i(L_i+w)}$ in W m^{-3} is the volumetric heating rate in the heating line. Therefore, Equation 4.2 requires knowledge of the spatially resolved temperature profile in the heating line, $\Delta T_{i,x}(x)$. From an analysis along the length of the heating line, it can be shown that

$$\Delta T_{i,x}(x<0) = -\frac{\dot{q}'''}{2\kappa_i}x^2 + \left[-\frac{\dot{q}'''}{2\kappa_i}(L_i+2w) + \frac{\Delta T_i}{L_i}\right]x + \left[-\frac{\dot{q}'''}{2\kappa_i}(w^2+L_iw) + \Delta T_i\left(\frac{L_i+w}{L_i}\right)\right]$$

$$\Delta T_{i,x}(x>0) = -\frac{\dot{q}'''}{2\kappa_i}x^2 + \left[\frac{\dot{q}'''}{2\kappa_i}(L_i+2w) - \frac{\Delta T_i}{L_i}\right]x + \left[-\frac{\dot{q}'''}{2\kappa_i}(w^2+L_iw) + \Delta T_i\left(\frac{L_i+w}{L_i}\right)\right]$$

Equation 4.3

where ΔT_i is the temperature rise at the heating line/sample contact. The thermal profile for the i^{th} heating line is shown in Figure 4.1(b). Equation 4.3 is then substituted into Equation 4.2 and subsequently equated with Equation 4.1 to give

$$Q_{in} = (IV)_i\left[\frac{L_i+2w}{2(L_i+w)}\right] - \frac{\Delta T_i}{R_{b_i}} = \sum_{j,j\neq i}\frac{\Delta T_{i,j}}{R_{b,j}} \qquad \textbf{Equation 4.4}$$

where I and V are the DC current and 4-probe voltage across the heating line, respectively. However, the experimental setup only provides a spatially averaged temperature of each line rather than the temperature at the metal/sample contact as required by Equation 4.4. For both heating and sensing lines, the contact temperature can be related to the measured average temperature of the line by

$$2(L+w)\,\overline{\Delta T}(x) = \int_{-(L+w)}^{+(L+w)}\Delta T(x)dx \qquad \textbf{Equation 4.5}$$

Because the thermal profiles in the sensing and heating lines are as shown in Figure 4.1(b), the contact temperatures are given by

$$\Delta T_i = \frac{2(L_i + w)}{L_i + 2w}\overline{\Delta T_i} - \frac{1}{6}(IV)_i\left[\frac{L_i^2}{(L_i + w)(L_i + 2w)}\right]R_{b,i}$$

$$\Delta T_j = \frac{2(L_j+w)}{L_j+2w}\overline{\Delta T_j} \qquad \textbf{Equation 4.6}$$

Finally, Equation 4.6 can be substituted into Equation 4.4 to express all terms as a function of known or measured quantities. It follows then that for any given heater line, *i*:

$$\sum_{j=1}^{3}\left[\frac{2(L_j+w)}{L_j+2w}\right]\left[\frac{\overline{\Delta T_j}}{(IV)_i}\right]G_{b,j} = \left[\frac{L_i+2w}{2(L_i+w)} + \frac{L_i^2}{6(L_i+w)(L_i+2w)}\right] \; for\; i = 1, 2, 3 \qquad \textbf{Equation 4.7}$$

where $G_b \equiv \frac{1}{R_b}$. The thermal circuit can then be solved by applying Equation 4.7 for each line acting as the heater to form a set of 3 linear equations with the 3 G_b as unknowns.

In an effort to reduce contamination of the signal by white or random noise, a fast Fourier transform (FFT) method developed by Fleming is used to determine all $\frac{\overline{\Delta T_{i,j}}}{(IV)_i}$ terms in Equation 4.7.[92] In brief, a discrete DC voltage stepped according to a sinusoidal function in time with frequency *f* is applied to the heater line, which induces a thermal signal at *2f* as shown in Figure 4.2. However, all of the measured signals are unavoidably contaminated by white noise and are therefore a linear combination of the true signal plus many random noise frequencies. To isolate the heating signal oscillating at 2*f*, we use a fast Fourier transform (FFT) algorithm in MATLAB to separate the total measured signal into its frequency components. An example of this process is shown in Figure 4.2, where

the time domain-signal of a sensing line is shown in (a) and the frequency-domain signal via FFT is shown in (b). The thermal response of the sensing line to the heating line input can clearly be seen above the noise at 2*f*, where the peak value corresponds to the amplitude of the time-domain oscillation.

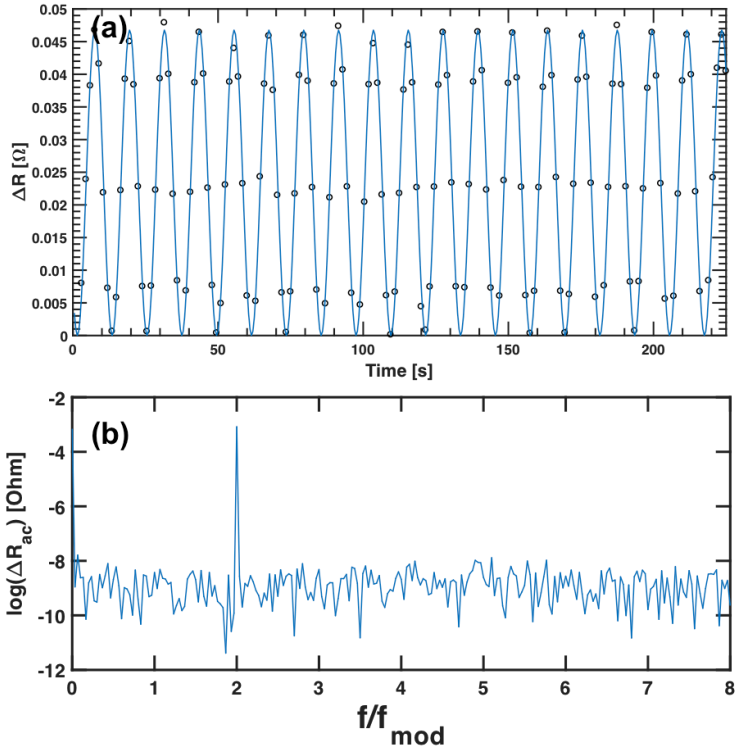

Figure 4.2: Example of (a) discrete time domain signal of a sensing line with a sinusoidal fit. The total signal is a linear combination of many frequencies, including the thermal response to the heating line and random noise contamination. (b) Frequency domain of the signal shown in (a). The FFT algorithm separates the time-domain signal into its frequency components where f_{mod} is the heating modulation frequency. The amplitude of the thermal signal oscillating at 2*f* is clearly seen above the noise.

The same process shown in Figure 4.2 is repeated to determine the first harmonic (1*f*) peak amplitude of the four-probe heating voltage (V_{DC}) and heating current (I_{DC}) and

the second harmonic ($2f$) modulation peak amplitude in the AC voltage amplitude of the sensing lines (ΔV_{ac}). Fleming showed that the final $\frac{\overline{\Delta T_{i,j}}}{(IV)_i} = \beta$ of the sensing lines is related to the measured signals by

$$\beta_{sense} = \frac{2\Delta V_{ac,2f}}{i_{ac}\left(\Delta V_{DC,1f} I_{DC,3f} + \Delta V_{DC,3f} I_{DC,1f} - \Delta V_{DC,1f} I_{DC,1f}\right)} \qquad \textbf{Equation 4.8}$$

where i_{ac} is the sensing current and is held constant by a large resistor in series with sensing lines. Similarly, β for the heating line can be found from[92]

$$\beta_{heat} = 4\frac{I_{3f} R_o - \Delta V_{DC,3f}}{R_o I_{1f}\left(I_{DC,1f} - I_{DC,3f}\right)^2} \qquad \textbf{Equation 4.9}$$

where $R_o = \frac{\Delta V_{DC,1f} + 3\Delta V_{DC,3f}}{I_{DC,1f} + 3I_{DC,3f}}$. The β values found from Equation 4.8 and Equation 4.9 are then plugged into Equation 4.7 to solve for the thermal conductance of each supporting beam.

With the sample contact temperatures and beam conductances calculated in Equation 4.6 and Equation 4.7, respectively, the graphene thermal conductivity can be calculated as

$$G_{S1} = \frac{Q_{2,1}}{\Delta T_2 - \Delta T_1} = \frac{\Delta T_1 G_{b,1}}{\Delta T_2 - \Delta T_1}$$

$$G_{S3} = \frac{Q_{2,3}}{\Delta T_2 - \Delta T_3} = \frac{\Delta T_3 G_{b,3}}{\Delta T_2 - \Delta T_3}$$

$$\kappa_{gr} = \left(G_{S1} - \alpha G_{S3}\right) \cdot \frac{L_{gr}}{t_{gr} \cdot w_{gr}} \qquad \textbf{Equation 4.10}$$

Where $\alpha \equiv \frac{L_3}{L_1}$ accounts for the difference in the section lengths due to EBL misalignment. The major assumption in Equation 4.10 is that the sample sections under study are symmetric, the only difference being the addition of graphene in one and not

the other. Such an assumption is valid since both the SiN_x bridge and *h*-BN flakes connecting the two sections are continuous materials.

4.2.2 Thermal Design for Signal Maximization in High Conductance Samples

Because the thickness of graphene considered here is small relative to that of *h*-BN, the difference in sample conductance can be very small. As a result, while measuring each sample section conductance is straightforward, determining the graphene thermal conductivity by calculating their difference as in Equation 4.10 accurately is still challenging. For example, if the thermal design of the device is not optimized, a 20% difference in thermal conductance may only result in a < 1% difference between the measured thermal signals, $\overline{\Delta T_1}$ and $\overline{\Delta T_3}$. A thorough thermal analysis of the device and careful design is therefore required to ensure a measureable signal. The following derivation assumes that line 2 acts as the heater line.

The experimental signal strength can be expressed as

$$\frac{\overline{\Delta T_1}-\overline{\Delta T_3}}{\overline{\Delta T_2}} = \frac{\Delta T_1-\Delta T_3}{\Delta T_2+\frac{1}{6}(IV)\left(\frac{L}{L+2w}\right)R_{b2}} \qquad \textbf{Equation 4.11}$$

where Equation 4.6 has been used to relate the measured average temperatures to the contact temperatures. Furthermore, the thermal circuit shown in Figure 4.1 can be used to show that

$$\Delta T_1 = \frac{R_{b1}}{R_{b1}+R_{s1}}\Delta T_2 \text{ and } \Delta T_3 = \frac{R_{b3}}{R_{b3}+R_{s3}}\Delta T_2 \qquad \textbf{Equation 4.12}$$

The contact temperature rise in the heater line can also be found from the thermal circuit in Figure 4.1 by summing the heat flow at the ΔT_2 junction such that

$$(IV) = \Delta T_2\left[\frac{1}{R_{b1}+R_{s1}}+\frac{1}{R_{b3}+R_{s3}}\right] - 2\kappa A\frac{d\Delta T_i(x)}{dx}\Big|_{x=L+w} \qquad \textbf{Equation 4.13}$$

where $\Delta T_i(x)$ is expressed in Equation 4.3. The exact solution for the measured signal strength can then be found by solving for ΔT_2 in Equation 4.13 and subsequent substitution into Equation 4.12 and Equation 4.11. An example of the effect of beam conductance on the measured signal for a typical experimental applied power of 50 μW is shown in Figure 4.3, which shows that the signal is maximized when $R_b \approx R_s$. Figure 4.3 also shows that for an improperly designed thermal structure where $R_b >> R_s$ or $R_b << R_s$, the signal can in fact vanish to *0*.

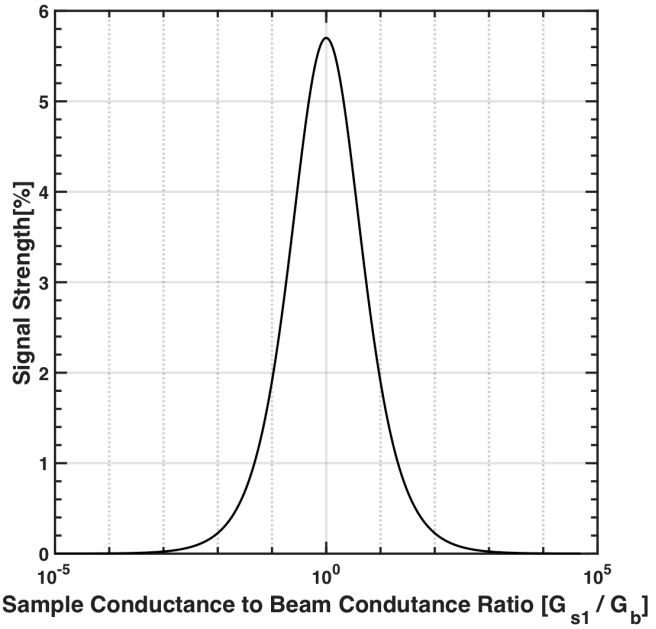

Figure 4.3: Example of an expected measured signal strength as a function of the beam to sample thermal resistance ratio. Typical experimental values for the beam geometry, applied power, and thermal conductivities of the *h*-BN, graphene, and beams were assumed.

In a slightly different analysis, the signal strength can be calculated from the thermal circuit as

$$\frac{\Delta T_1 - \Delta T_3}{\Delta T_2} = \frac{R_{b1}}{R_{b1} + R_{s1}} - \frac{R_{b3}}{R_{b3} + R_{s3}} = \frac{R_{b1}(R_{b3} + R_{s3}) - R_{b3}(R_{b1} + R_{s1})}{(R_{b1} + R_{s1})(R_{b3} + R_{s3})}$$

Equation 4.14

For similar beam geometries and small differences in R_{s1} and R_{s3}, Equation 4.14 can be simplified to

$$\frac{\Delta T_1 - \Delta T_3}{\Delta T_2} \approx \frac{R_b}{(R_b + R_s)^2}(R_{s1} - R_{s3}) \qquad \textbf{Equation 4.15}$$

Finally, the R_b that maximizes the signal can be found by taking the partial derivative of Equation 4.15 with respect to R_b and setting it equal to *0*, which again gives $R_{b,max} \approx R_s$.

One approach to increasing the beam conductance to match the high sample conductance considered in this study is to use thick Au (130 nm) instead of Pd (80 nm) and SiN_x (500 nm) instead of SiO_2 (300 nm). Figure 4.4(b) shows the predicted beam resistances of these two cases assuming thermal conductivities of 125, 25, 4, and 1.3 W m^{-1} K^{-1} for the Au, Pd, SiN_x, and SiO_2, respectively. For ease of fabrication, it is desirable to have beam lengths ≥ 30 μm. While the thermal resistance is seen to drop by one order of magnitude as compared to Pd/SiO_2, the single Au beam on nitride is still larger than that of the graphene sample section, which is shown in gray for 1 to 15 layers of graphene. Furthermore, increasing the metal thickness any further would reduce the electrical resistance of the line to below 10 Ω, which would require excessively large heating currents during the measurement. As a result, the device used in this study incorporated two extra auxiliary beams in parallel with the original three beams, as shown in Figure 4.4(a). These beams act to reduce the effective thermal resistance, $R_{b,eff}$, of the sample support beams to that of the graphene sample section, as shown in Figure 4.4(b). Experimental examples of the measured signal of a thermally poorly designed

device at 300 K using SiO_2/Pd beams (3 beams total) and an optimized device that incorporates auxiliary beams (5 beams total) consisting of SiN_x/Au are shown in Figure 4.5(a) and (b), respectively. In both configurations, the center-line acted as the heater.

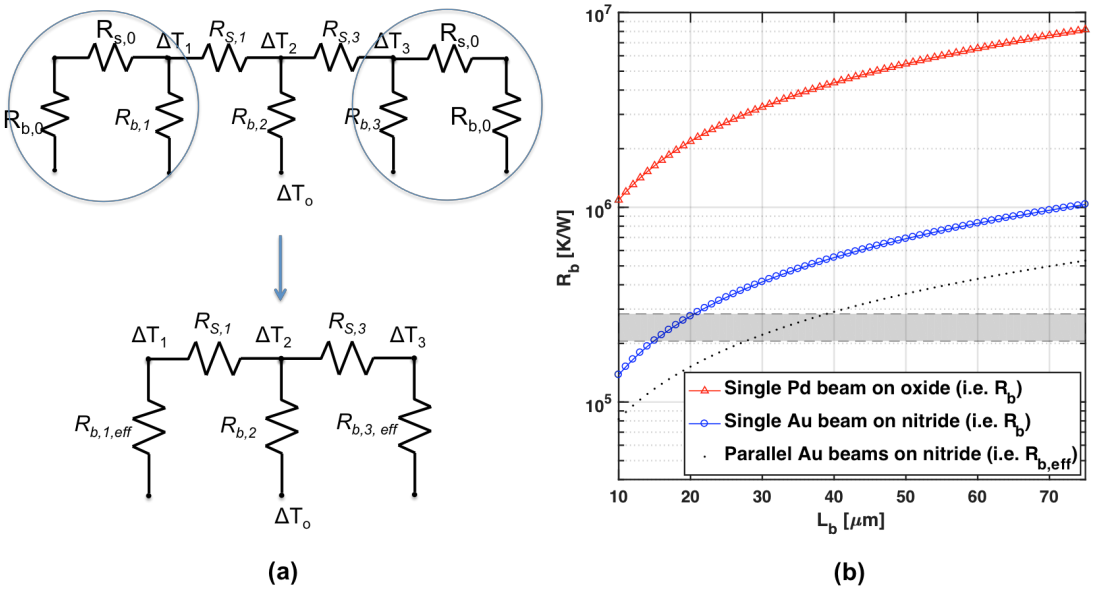

Figure 4.4: (a) Modified thermal circuit, which adds auxiliary heat transfer beams in parallel with the original design to reduce the effective thermal resistance of the beams. (b) Calculated thermal resistance of various device configurations. The shaded gray region is the predicted thermal resistance of the graphene sample section for 1 to 15 layers of graphene.

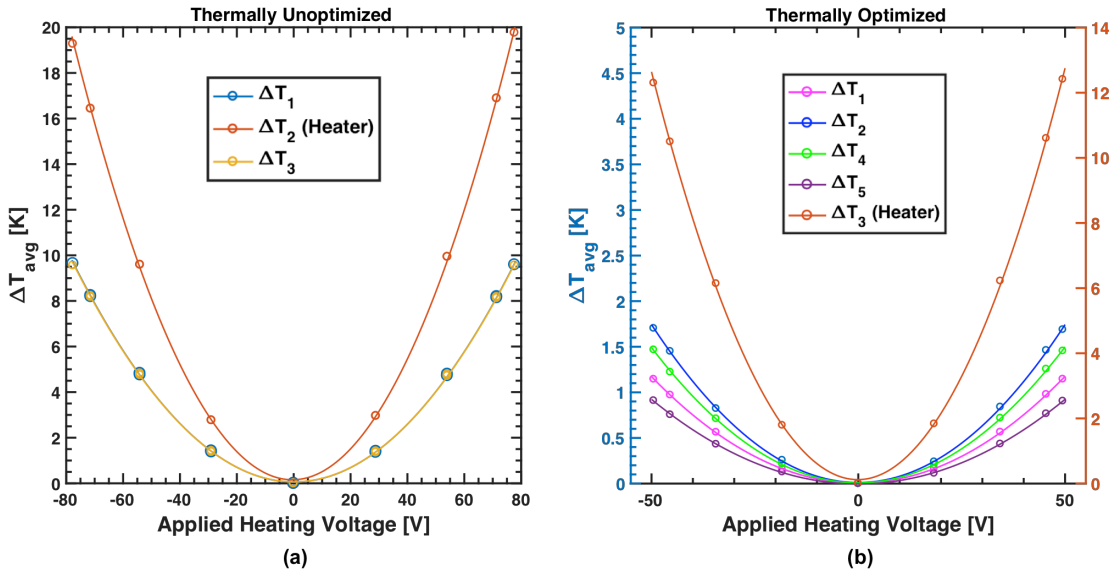

Figure 4.5: Examples of (a) a poor thermal design representative of the schematic shown in **Figure 4.1** with Pd/SiO_2 support beams (3 total) where $R_b >> R_s$ such that $\Delta T_1 \approx \Delta T_3$ forcing the signal to *0*. (b) An optimal thermal design as shown in Figure 4.4 with auxiliary support beams made of Au/SiN_x (5 beams total). A clear difference in the contact temperatures can be measured.

For the designs considered here, R_{sp} is approximately 3×10^3 K W^{-1}, which is two orders of magnitude smaller than the Au/SiN_x resistance such that the temperature rise at the beam root can be assumed to be *0*.

4.5 Device Fabrication

The methods used in fabricating the sample are outlined in this section. First, the polymer-free dry transfer method is described in some detail here, but a more in depth discussion using the same equipment can be found in the works of Kim et. al.[87] The microfabrication process of the final suspended structure is then outlined in detail.

4.5.1 Clean Dry-Transfer and Heterostructure Stacking using a Hemispherical Stamp

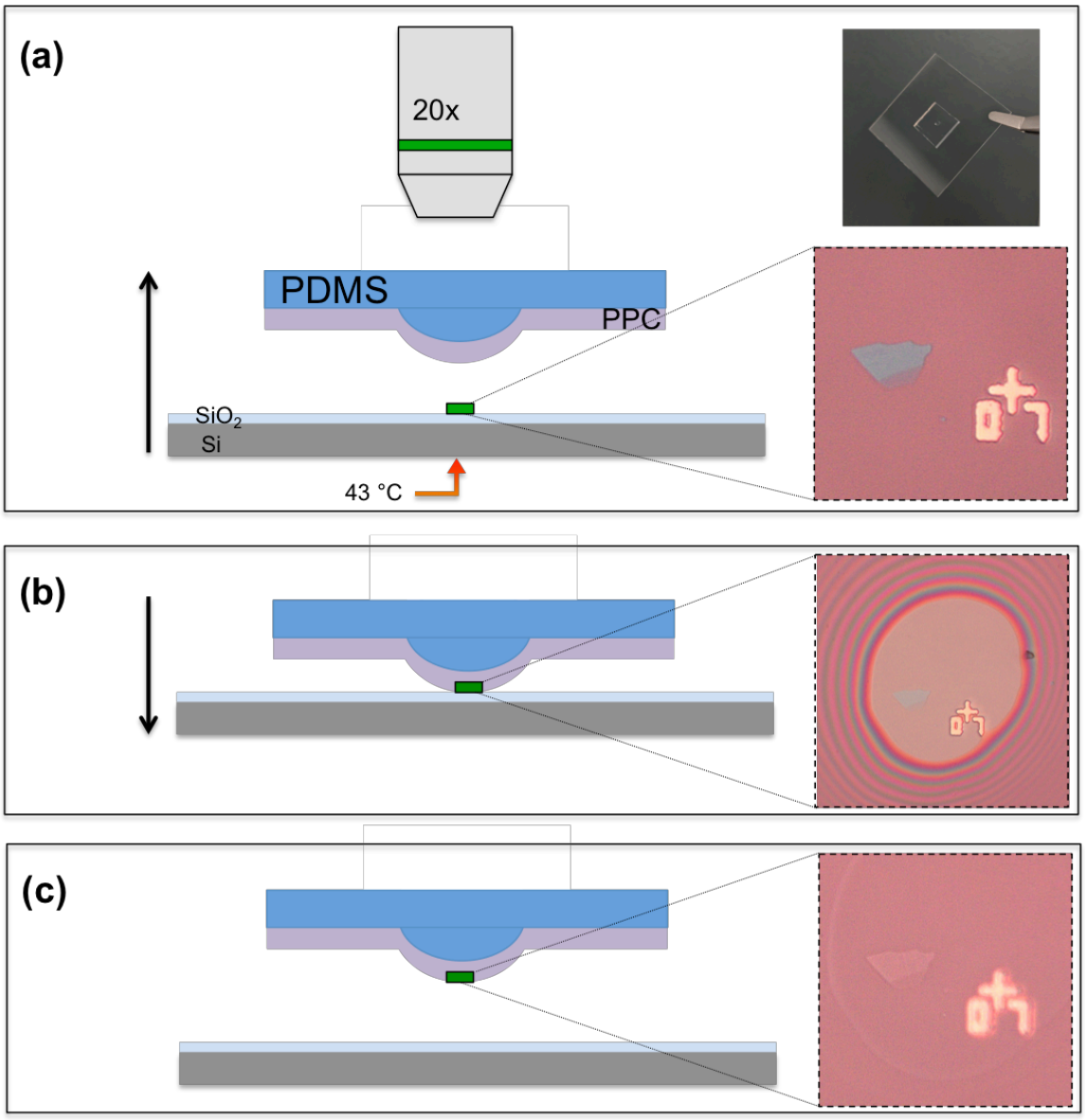

Figure 4.6: (a) The schematic shows the heated substrate via the custom chuck, which is raised slowly to make contact with the PDMS/PPC stamp. Optical image on top-right shows the PDMS stamp on a square glass coverslip. Optical image on bottom-right is the flake as seen through the transparent PDMS/PPC stamp. Top right image shows the PDMS/PPC stamp mounted to a square glass microscope cover slip. (b) Contact between

sample and stamp is made. The stage is then quickly lowered to pop the sample off of the substrate surface. The inset shows the area of contact with the stamp, where the rainbow fringes are parts of the stamp not in contact with the sample. (c) After dropping the sample chuck quickly, the sample detaches from the surface and sticks to the PPC. The flake appears transparent in the optical image.

The same hexagonal boron nitride source as that used in Chapter 3 was used in this study. The graphene was exfoliated from a natural graphite source. Both *h*-BN and graphene flakes were exfoliated using blue cleanroom tape onto 300 nm oxidized silicon for identification via optical contrast. The final thicknesses of the top *h*-BN, graphene, and bottom *h*-BN flakes were measured by AFM to be 20 nm, 3.7 nm, and 10 nm respectively.

In order to ensure completely residue-free graphene, a dry transfer process was used to create the final heterostructure stack.[87] A hemispherical stamp was first made by curing a ~1 mm diameter drop of PDMS on top of an already cured PDMS strip, as shown in the optical image of Figure 4.6(a). A thin layer of 15% by mass polypropylene carbonate (PPC) in anisole is then spun on the hemisphere at 4000 rpm for 50s and baked on a hot plate set to 180 °C for 3 minutes. Alternatively, PPC that has already been spun and cured on a smooth PDMS mold can be mechanically peeled, placed onto the hemispherical PDMS stamp, and baked at 180 °C such that the hemispherical PDMS stamp can be reused indefinitely. The PDMS/PPC stamp is then placed on a glass slide and mounted hemisphere-side down onto the mask chuck of a photolithography mask aligner (Karl Suss MJB4 Mask Aligner) as shown in Figure 4.6(a).

Before pick-up, the target flakes were baked in a box furnace at 340 °C under high-vacuum (3×10^{-7} Torr) for 8 hours to drive off surface adsorbants and any moisture between the flake and substrate to allow for easier release from the substrate. Immediately after removal from the furnace, the substrate containing the target flake for pick-up is mounted onto a custom temperature-controlled sample chuck. The small diameter of the hemisphere and fine vertical control of the mask aligner stage allows for selective pick-up of flakes with micrometer precision. The sample chuck is then heated to 43 °C and the flake is brought into contact with the PDMS/PPC stamp, as shown in Figure 4.6(b), where the optical image shows the area of contact between the stamp and flake. At this temperature, the vdW force between the PPC and *h*-BN is stronger than the vdW force between the flake and SiO_2, which allows for the detachment of the sample from the substrate when the chuck is lowered quickly as is shown in Figure 4.6(c). The detached flake appears optically transparent. It was found that the quick speed at which the flake is released was imperative, with the picking-up of the flake best described as a pop, snap, or plucking off the surface. To release the flake onto the next layer of the heterostructure, the sample is brought into contact with the target area at room temperature. The chuck temperature is then raised to 90 °C and the stage is very slowly lowered, detaching the flake from the PPC. Similar to the pick-up process, the slow speed at which the chuck was lowered was critical to improving yield, which opposite to the pick-up motion is best described as a slow peeling back of the PPC. To improve contact between layers, the stack is then baked again at 340 °C under high-vacuum overnight. The process is repeated until all layers of the heterostructure have been stacked and transferred to the final SiN_x substrate.

4.5.2 Microfabrication of the Final Suspended Device

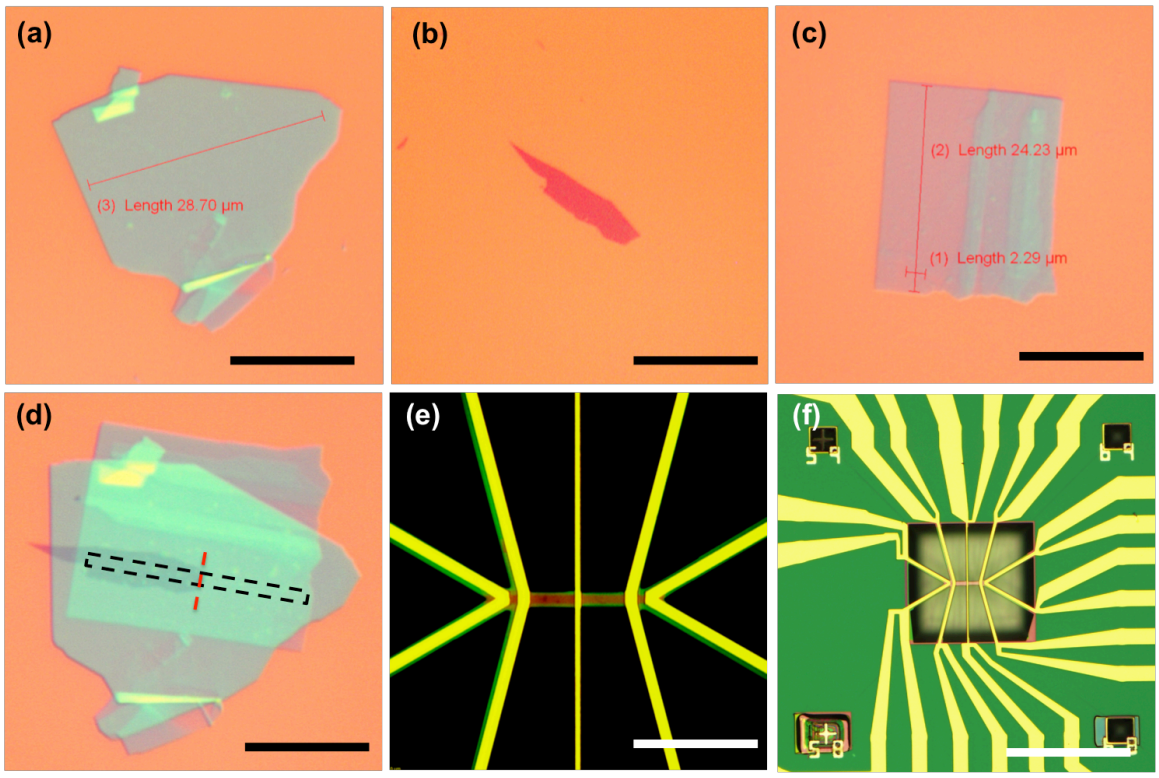

Figure 4.7: (a) Top h-BN, (b) MLG, and (c) bottom h-BN flakes as exfoliated onto 300 nm thick SiO_2. (d) The final heterostructure stack on SiO_2 before transfer to SiN_x. An outline of the final sample sections is shown by the black dashed lines. The red dashed line marks the border between the *h*-BN/graphene/*h*-BN section to the left and the *h*-BN/*h*-BN section to the right as shown in (e) High-contrast optical image of the final suspended device. The graphene can be identified in the left sample section by the darker red color. (e) Reduced magnification optical image to show the suspended configuration. The scale bars in (a)-(d) are 15 µm, while the scales in (e) and (f) are 20 µm and 100 µm, respectively.

After the final heterostructure stack was transferred to the SiN_x substrate, PMMA was spun on the substrate at 3000 rpm for 50s and baked at 180 °C for 2 min. Electron

beam lithography was then used to define a 1.5 μm wide, 26 μm long rectangular section centered at the boundary between *h*-BN/graphene/*h*-BN and *h*-BN/*h*-BN sections. After developing the PMMA in 1:3 MIBK:IPA for 25s, the uncovered portions of the heterostructure were etched in a 40 mTorr CHF_3 (40 sccm) and O_2 (3 sccm) plasma at 400 DC power for 45 seconds. After stripping the PMMA etch mask in 75 °C acetone for 2 hours, a fresh PMMA layer was spun on the substrate and a second EBL step was used to define the metal leads, heater lines, and bonding pads. An 8.2 nm Cr adhesion layer was then deposited using an e-beam metal evaporator. As determined in Section 4.3, 133 nm of gold was deposited to ensure the effective thermal resistance of the beams was similar in magnitude to the thermal resistance of the sample sections. Metal liftoff was achieved via a 45 minute soak in 70 °C acetone. For eventual suspension of the final device, the 500 nm thick SiN_x surrounding the device needed to be etched. Due to this large thickness, ZEP 520A instead of PMMA was used as an etch mask due to its higher resistance to plasma etching. However, PMMA was still used as a sacrificial release layer between the ZEP and nitride since complete removal of ZEP post-etching was found to be quite difficult. The ZEP layer was spun on top of the PMMA at 2000 rpm for 60s, baked at 180 °C for 2 minutes, and exposed in a third EBL step. After development in Amyl-Acetate for 2 minutes, the uncovered portions of nitride were etched in 2 minute intervals for 14 total minutes in a 175 W CF_4 (25 sccm, 30 mTorr) plasma. The resist was then stripped in remover PG set to 105 °C for 2 hours. The sample was then submerged in 5% HF for 30s to remove the native oxide, rinsed in cold DI water, and then immediately submerged in 4% tetramethylammonium hydroxide (TMAH) on a hot

plate set to 105 °C for 25 minutes. The TMAH bath at this hot plate temperature is estimated to be ~80°C.

The final device was then mounted to a chip carrier and electrical connections were made to the sample using a wirebonder. Measurements were carried out in a cryostat under vacuum.

4.6 Results and Discussion

Figure 4.8 shows the measured thermal conductivity of the 11-layer graphene encased in *h*-BN of this work (yellow filled stars) along with the thermal conductivity of graphene supported on SiO_2 measured by Sadeghi and coworkers (open diamonds) and graphene encased in SiO_2 measured by Jang and coworkers (open squares).[86,93] For similar layer thicknesses, the thermal conductivity of *h*-BN encased graphene was shown to be much higher than SiO_2-supported and encased graphene. The peak thermal conductivity of the device in this work is $996 \pm {}^{101}/_{47}$ W m^{-1} K^{-1}, which is comparable to the 34-layer SiO_2-supported graphene and nearly double that of the 14-layer SiO_2-encased graphene. The measured AFM thickness of the MLG flake represents the upper limit on the graphene thickness.[94] As a result, the asymmetric uncertainty is a result of a considered MLG thickness ranging from 10-11 layers. Equally as important, the peak thermal conductivity of the device in this study is down shifted to ~ 200 K, whereas the peak for SiO_2-supported and encased graphene for < 27 layers occurs at ~250-300 K. Because the thermal conductivity of supported graphene increases with increasing thickness, the results suggest that the *h*-BN enhances thermal transport in MLG.[86,93] To better understand the comparative results in Figure 4.8, it is important to discuss the possible mechanisms that could be responsible for the higher thermal conductivity and lower-

temperature peak position seen in our data. To this end, it is instructive to re-examine the experimental and theoretical works presented in the literature, where several different mechanisms have been the proposed.

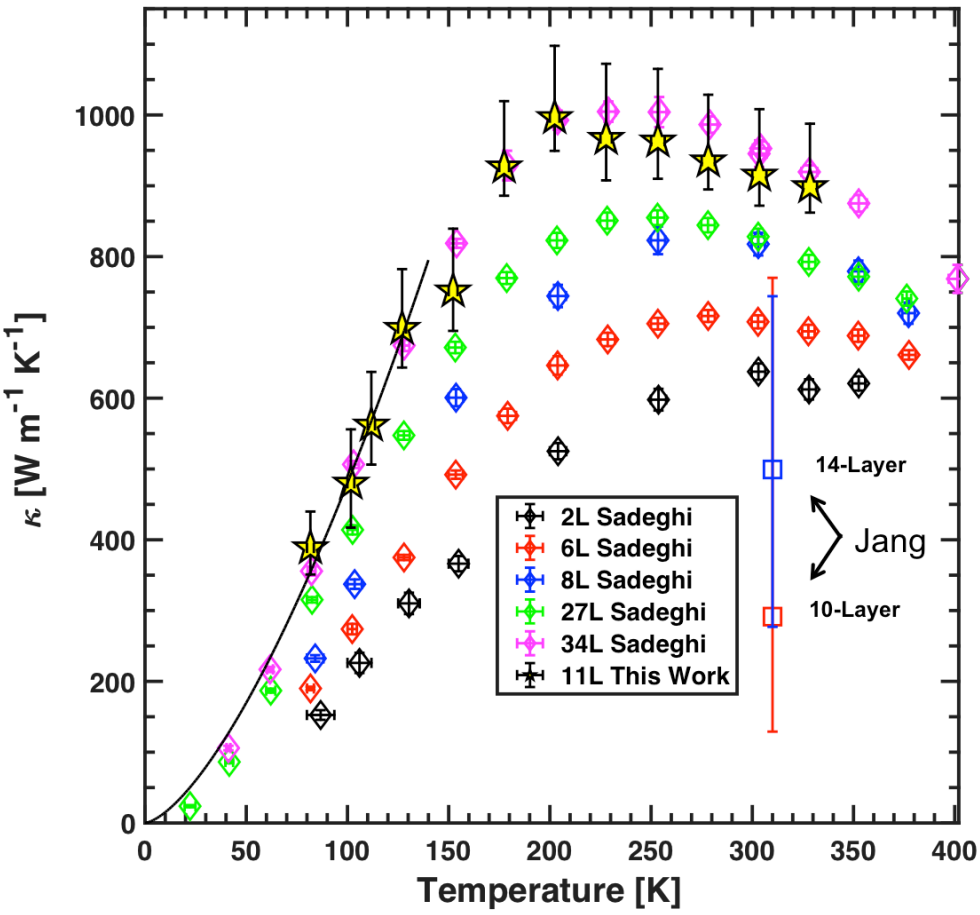

Figure 4.8: Measured thermal conductivity of the 11 layer graphene sample encased in *h*-BN of this study (yellow filled stars) plotted with the thermal conductivity of multilayer graphene supported on SiO_2 measured by Sadeghi et. al. and encased in SiO_2 measured by Jang et. al.[86,93] The dashed black line shows the low-temperature dependence of $\kappa \propto T^{1.7}$.

First, point defects in the graphene introduced during the fabrication process could affect thermal transport. However, a Raman spectroscopy analysis on all of the oxide-supported samples by Sadeghi and coworkers did not show the emergence of the D-peak commonly associated with defects.[86] In the same vein, lateral boundary scattering due to edge roughness caused by plasma etching could contribute to a reduced basal-plane thermal conductivity. To this end Sadeghi and coworkers calculated the theoretical thermal conductivity of their ~3 μm wide graphene sample assuming that lateral scattering was dominant. The calculation revealed that κ_{calc} was actually much higher than κ_{meas}.[41,86] Therefore, the authors reasoned that edge roughness could not be the dominant scattering mechanism in their samples. Additionally, the width of the sample considered in this study was only 1.3 μm. Lateral boundary scattering therefore also cannot be a major contributing factor in describing the observed differences between the two studies. Finally, since the graphene flakes in this study were exfoliated from the same source as that by Sadeghi and coworkers, intrinsic differences between the graphene samples are small. Instead, it is likely that the enhanced transport shown in Figure 4.8 stems from extrinsic differences between the oxide and *h*-BN interactions with graphene.

Strong graphene-substrate bonding to Ni has previously been shown to modify the dispersion relation of SLG, while intercalation of Cu between the SLG and Ni was seen to recover the pure graphene dispersion.[95] This difference in behavior was attributed to a weaker bonding at the Cu interface than at the Ni interface. Since the adhesion energy of SLG/Cu was measured to be 0.72 J m^{-2},[96] which is higher than the measured SLG/SiO_2 and MLG/SiO_2 adhesion energies of 0.45 and 0.31 J m^{-2},[97] respectively, Sadeghi and coworkers concluded that modification to the dispersion relation was not the reason for

the observed thickness-dependent behavior of their samples.[86,93] Similarly, the adhesion energy of graphene to *h*-BN has been calculated to be on the order of 0.22 J m^{-2} and is therefore not expected to appreciably alter the phonon dispersion of MLG either.[82,98]

In another study, SLG was shown to conform closely to its support substrate.[99] Consequently, the difference in atomic roughness of SiO_2 compared to atomically smooth *h*-BN had been proposed as one mechanism responsible for reduced electronic transport in oxide supported graphene.[10,65] Analogous to electronic transport, oxide surface roughness can result in scattering centers for phonons. However, the roughness at the graphene surface induced by the oxide in SLG strongly saturates with increasing layer thickness, where surface corrugations of supported MLG beyond 3-layers approach the amplitude and wavelength of intrinsic ripples in suspended SLG.[86] AFM measurements have shown a reduced surface roughness from 185 pm for SLG to 127 pm for 15-layer graphene with an extrapolated roughness of 123 pm for bulk graphite supported on oxide.[97] The effect of roughness therefore does not penetrate beyond the first few layers. Furthermore, the oxide roughness at the interface primarily scatters high-frequency phonons rather than the low-frequency phonons that are thought to dominate the thermal conductivity in suspended SLG. Regardless, even if the oxide surface were atomically smooth, we would still not expect the thermal conductivity of the supported graphene to be significantly improved. This notion will be discussed in further detail later.

The preceding discussion suggests that the observed trend in Figure 4.8 requires an inspection of the interaction between the thermal energy carriers in graphene and its substrate at a more fundamental level. To this end, an overview of the dominant thermal carriers in graphene would be helpful. Although it is a semi-metal, the thermal

conductivity of isolated graphene is dominated by phonons rather than electrons, with an upper-bound on the electronic contribution of ~10% of the total κ at room temperature.[36,100,101] The anomalously high lattice contribution is attributed to the unique dispersion relation of graphene, which contains three low-frequency acoustic modes and three high-frequency optical modes. Due to their high energies and low group-velocities, the three optical modes do not contribute significantly to the thermal conductivity except at high temperatures.[85] In contrast, the low-ω acoustic modes contribute significantly to κ at room temperature and below, due to longer mean free paths, λ, and larger populations, $N = f_o(\omega) \cdot D(\omega)$, where $f_o(\omega)$ is the equilibrium Bose-Einstein distribution function and $D(\omega)$ is the 2D density of states in graphene.[40,85] The in-plane longitudinal acoustic (LA) and transverse acoustic (TA) modes exhibit an approximately linear relationship between frequency, ω, and wave vector, $\vec{k}$, while the out-of-plane flexural acoustic (ZA) mode has an unusual quadratic relation near the Brillouin zone (BZ) center. Due to its quadratic dispersion, the ZA phonon density of states is constant while the LA and TA density of states vanishes as ω approaches 0.[40,85] Furthermore, the frequencies of ZA modes remain much lower than the TA and LA frequencies even near the zone boundary. As a result, the number density of flexural modes are nine-fold and twenty-fold more populated than the TA and LA modes, respectively, at room temperature and remain more populated at the zone boundary at high temperatures.[85] In addition, while the linear LA and TA modes have relatively large group velocities compared to the ZA mode near the zone center, near the zone boundary the velocity of the ZA mode becomes appreciable. Lastly, Lindsay *et al*. showed through a rigorous exact numerical solution of the Boltzmann transport equation (BTE) that the flexural modes in isolated SLG are subject to a

reflection symmetry rule that significantly reduces their phonon-phonon scattering phase space. In other words, in single-layer suspended graphene, the ZA mode phonons are significantly less likely to undergo Umklapp scattering, the mechanism responsible for the intrinsic thermal resistance of a material. As a result of the disproportionately large phonon population and reduced probability of Umklapp scattering, the flexural modes contribute significantly to the intrinsic thermal conductivity of suspended SLG and can account for up to 77% of the total κ at room temperature.[85] Naturally, it follows that extreme deviation of κ in supported SLG and MLG is likely a manifestation of suppressed contributions from these low-frequency modes.[16]

Unlike interface roughness and defect scattering which preferentially scatter high frequency phonons, the transmission of phonons across an interface, scales as ω^{-2}.[100,102] Consequently, the low-frequency phonons in graphene are more susceptible to being transmitted across the interface and lost to the support material.[17] Indeed, this phenomenon was calculated by Sadeghi and co-workers where experimental interface conductance values were used to show that the average transmission coefficient increases with decreasing temperature. In turn, a higher average transmission at lower temperature suggests that the interface has a pronounced influence on the low-frequency modes since the overwhelming majority of thermally excited phonons at low-temperature are those with low-frequencies. A similar sentiment was echoed in the works of Jang and co-workers who used a phenomenological model to show that the influence of an oxide substrate penetrates several nanometers into MLG flakes and that this penetration depth increased with decreasing temperature.[93] Moreover, the average mean free path of phonons along the *c*-axis direction has previously been calculated to be large as 20 nm

(or 60 atomic layers) in MLG at room temperature and over 300 nm at temperatures below 70 K.[86] This suggests that phonons emerging from one interface can traverse to the other without scattering. It is therefore conceivable that interface phonon leakage can lead to a reduced thermal conductivity even for relatively thick MLG samples. The data in Figure 4.8 supports this notion and shows that κ of supported MLG decreases with decreasing layer thickness.

The effect of phonon leakage across the *h*-BN/substrate boundary is also related to the temperature dependent location of the peak. In the most general case, the specific heat of a material, C_p, can be calculated as

$$C_{p,ph} = \int_0^{\omega_{max}} k_b \left(\frac{\hbar\omega}{k_b T}\right)^2 \frac{e^{\left(\frac{\hbar\omega}{k_b T}\right)} D(\omega)}{\left(e^{\left(\frac{\hbar\omega}{k_b T}\right)} - 1\right)^2} d\omega \qquad \textbf{Equation 4.16}$$

where $\hbar$ and k_b are the reduced Planck's constant and Boltzmann constant, respectively.[103] Unlike the specific heat, which is a measure of the energy stored in the thermally excited phonons, thermal conductivity is a transport property that measures the relative ease with which the phonons move throughout the lattice. The two properties are related by $\kappa = \sum_p \sum_{\vec{k}} C_p \cdot \vec{v} \cdot \lambda_{eff}$, where $\vec{v}$ and λ_{eff} are the average phonon velocity and effective mean free path, respectively. In turn, the effective mean free path follows Matthiessen's rule such that

$$\frac{1}{\lambda_{eff}} = \frac{1}{\lambda_{intrinsic}} + \frac{1}{\lambda_{extrinsic}} \qquad \textbf{Equation 4.17}$$

where $\lambda_{intrinsic}^{-1}$ scales with temperature and $\lambda_{extrinsic}^{-1}$ is comparatively less sensitive to temperature. In the low-temperature boundary-scattering regime $\lambda_{extrinsic} \ll \lambda_{intrinsic}$. As such, the effective mean free path is not very sensitive to temperature and κ scales

approximately with C_p. As the temperature continues to increase and more phonons become populated, they begin to scatter with one another. Known as Umklapp scattering, the mean free path of this intrinsic mechanism scales as $\lambda_U \propto T^{-1}\omega^{-2}$ and destroys the forward momentum of the phonons.[86] The peak κ occurs where the intrinsic Umklapp mean free path becomes comparable to the extrinsic mean free path. A shift of the peak to higher temperatures is therefore indicative of relatively smaller $\lambda_{extrinsic}$ or, qualitatively, larger extrinsic phonon scattering.

In the specific case of graphene, boundary effects can be even more pronounced since low-ω ZA phonons are thought to dominate the intrinsic κ. This sentiment is reflected in the molecular dynamics simulation works of Z. Zhang, Mao, J. Zhang and coworkers, and Pak and Hwang who calculated that the low-frequency, out-of-plane vibrational phonons are significantly suppressed by a substrate via either high transmission across the interface or reduced phonon lifetimes.[15–18] This behavior is true for both *h*-BN and SiO_2, but with a stronger suppression in the oxide case. In contrast, the mean free path of the TA and LA modes at low-frequency were shown to be largely unaffected by *h*-BN.[18] The results can be interpreted as a shift in the relative importance of the TA and LA modes compared to the ZA mode in supported graphene.

The data in Figure 4.8 reflects this phenomenon where κ_{peak} for *h*-BN encapsulated graphene occurs at ~ 200 K. In comparison, the κ_{peak} for similar thickness graphene supported by oxide, encased in oxide, and even suspended but polymer-contaminated graphene occurs at ~ 250-300 K.[14,41,86,93] Significantly, at the lowest temperature measured in this study the measured conductivity of our 11-layer sample is larger than even the 34-layer SiO_2 supported sample and even larger still than the similar-thickness

8-layer sample on oxide. We therefore conclude that the *h*-BN support causes less extrinsic scattering and leakage compared to oxide-supported and polymer-contaminated samples.

In this discussion of phonon leakage, it is important to note that phonons leaking from the graphene to the substrate must be replaced by an equal interface heat flux carried by phonons leaking from the substrate to the graphene. This arises from a net-zero net interface heat flux condition across the boundary since the applied temperature gradient is parallel to the interface. Phonons arising from an amorphous substrate like SiO_2, however, are expected to be isotropic in the reciprocal space and therefore contribute significantly less to κ than those originating from within the graphene itself. In the case of *h*-BN where the layers are crystalline and similar in structure to that of graphene, the exchange of diffusive phonons from the support to the MLG should be reduced. In a fully first principles Landauer approach, Mao et. al. calculated a room temperature thermal conductance of ~ 2×10^8 W m^{-2} K^{-1} for epitaxially aligned graphene on *h*-BN,[17] which is similar to the measured thermal conductance of polymer-free graphene on oxide of 1.8×10^8 W m^{-2} K^{-1} at 300 K[79]. The difference between the two substrates therefore likely lies in the nature of the phonons emerging from the dielectric at the boundary, where a larger majority of phonons from *h*-BN resemble a specular exchange rather than a diffuse one like from the oxide.[86]

To better illustrate the effect of the substrate on phonon leakage, the heat flux through the sample can be calculated as

$$q_x''(y) = \frac{1}{\forall}\sum_p \sum_{\vec{k}} g\hbar\omega v_X \qquad \textbf{Equation 4.18}$$

where ∀ is the volume of the graphene sample, p and $\vec{k}$ are the polarization and wave-vector of a phonon, respectively, $g \equiv [(f(x,y) - f_o(x)]$is the deviation of the local distribution function from equilibrium, and v_x is the phonon group velocity in the *x*-direction. Assuming the relaxation time approximation, the steady-state Boltzmann transport equation (BTE) can be solved to obtain g

$$-\frac{g(x,y)}{\tau} = v_x \frac{\partial f(x,y)}{\partial x} + v_y \frac{\partial f(x,y)}{\partial y} \qquad \textbf{Equation 4.19}$$

where τ is the distribution relaxation time and the dependence on the *z*-direction has been dropped for the relatively large width of the sample considered in this study. Furthermore, $\frac{\partial f}{\partial y} = \frac{\partial g}{\partial y}$ since $f_o \neq \mathrm{f}(y)$, and for small deviations from equilibrium $\frac{\partial f}{\partial x} = \frac{\partial f_o}{\partial T}\frac{dT}{dx}$. Equation 4.19 can be rewritten as

$$-\tau v_y \frac{\partial g}{\partial y} - g = \tau v_x \frac{\partial f_o}{\partial T}\frac{dT}{dx} = S_o \qquad \textbf{Equation 4.20}$$

All terms on the right hand side are constant in *y*, such that they can be treated as a constant source term, S_o, in the solution of g, which has a general solution of the form

$$g_i(y) = C \cdot \exp\left(-\frac{y}{\tau_i v_i \cdot cos\theta_i}\right) - S_{o,i} \qquad \textbf{Equation 4.21}$$

where the subscript *i=1* for graphene, *i=2* for the support and θ_i is defined in Figure 4.9.

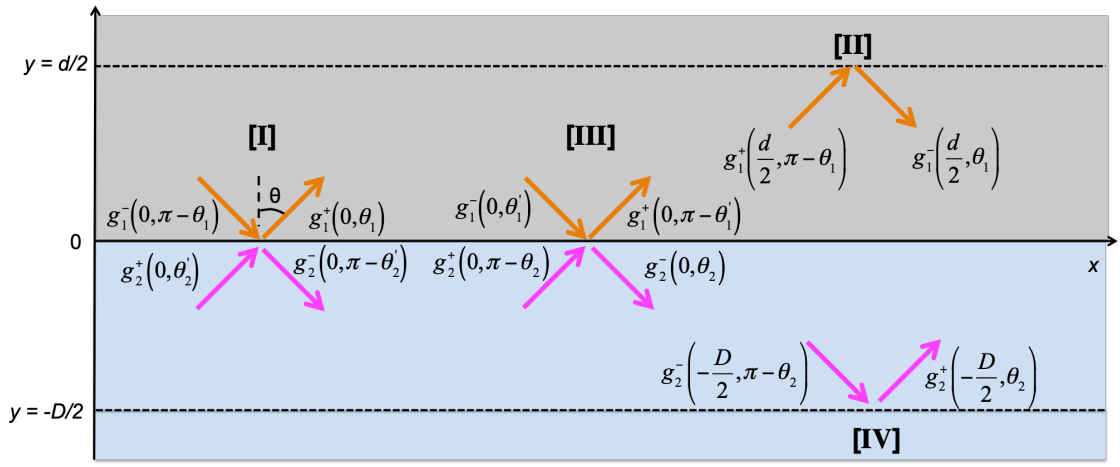

Figure 4.9: The super-lattice coordinate system defined for solution of the BTE for graphene and its support. The dotted lines represent symmetry planes. The blue shaded region represents the support material while the gray space region represents the graphene layer.

We solve for the constants of integration, C, in Equation 4.21 for the super-lattice structure shown in Figure 4.9 with alternating graphene and *h*-BN layers. The four geometric regimes considered are:

$$(1)\ g_1^+(y,\theta_1) \rightarrow \left[0 < y < \frac{d}{2}\right]\ and\ \left[0 < \theta_1 < \frac{\pi}{2}\right]$$

$$(2)\ g_1^-(y,\theta_1) \rightarrow \left[0 < y < \frac{d}{2}\right]\ and\ \left[\frac{\pi}{2} < \theta_1 < \pi\right]$$

$$(3)\ g_2^+(y,\theta_2) \rightarrow \left[-\frac{D}{2} < y < 0\right] and\ \left[0 < \theta_2 < \frac{\pi}{2}\right]$$

$$(4)\ g_2^-(y,\theta_2) \rightarrow \left[-\frac{D}{2} < y < 0\right]\ and\ \left[\frac{\pi}{2} < \theta_2 < \pi\right] \qquad \textbf{Equation 4.22}$$

where d and D are the thickness of the graphene and support layer, respectively, and the g^+ or g^- notations represent phonons moving in positive or negative y-direction, respectively. The boundary conditions for Equation 4.22 shown in Figure 4.9 and are given as:

$$[I]\ g_1^+(0,\theta_1) = (1-T_{12})P_{1R}g_1^-(0,\pi-\theta_1) + T_{21}P_{2T}g_2^+(0,\theta_2')$$

$$[II]\ g_1^-\left(\frac{d}{2},\theta_1\right) = g_1^+\left(\frac{d}{2},\theta_1\right)$$

$$[III]\ g_2^- = (0,\theta_2) = (1-T_{21})P_{2R}g_2^+(0,\pi-\theta_2) + T_{12}P_{1T}g_1^-(0,\theta_1')$$

$$[IV]\ g_2^+\left(-\frac{D}{2},\theta_2\right) = g_2^-\left(-\frac{D}{2},\theta_2\right) \qquad \textbf{Equation 4.23}$$

where $0 < P < 1$ is a specularity parameter that quantifies the probability that an incoming phonon will undergo a mirror-like reflection, $0 < T_{ij} < 1$ is the transmission coefficient of the incident phonon from material *i* to material *j*, and the subscripts *R* and *T* denote reflection or transmission. Equation 4.21 can be solved using the boundary conditions in Equation 4.23 to solve for the constants *C* as

$$C_1^+ = \frac{[1-(1-T_{12})P_{1R}]S_{o1} + T_{21}P_{2T}[C_2^+ - S_{o2}]}{1-(1-T_{12})P_{1R}exp\left(\frac{d}{\tau_1 v_1 cos\theta_1}\right)}$$

$$C_1^- = C_1^+ exp\left(\frac{d}{\tau_1 v_1 cos\theta_1}\right)$$

$$C_2^- = \frac{[1-(1-T_{21})P_{2R}]S_{o2} + T_{12}P_{1T}[C_2 - S_{o1}]}{1-(1-T_{21})P_{2R}exp\left(-\frac{D}{\tau_2 v_2 cos\theta_2}\right)}$$

$$C_2^+ = C_2^{-1}exp\left(-\frac{D}{\tau_2 v_2 cos\theta_2}\right) \qquad \textbf{Equation 4.24}$$

A few limiting solutions for Equation 4.24 are:

(a) [$P_i = 1$, $T_{ij} = 0$], Non-interacting materials, atomically smooth boundaries

(b) [$P_i = 0$, $T_{ij} = 0$], Non-interacting materials, diffusely scattering boundaries

(c) [$P_i = 1$, $T_{ij} = 1$, $\tau_1 = \tau_2$, $v_1 = v_2$], Material 1 = Material 2

(d) [$\tau_2 = 0$, $P_i = 1$, $0 < T_{ij} < 1$], Highly disordered support with a smooth interface

For limiting cases (a) and (b), the constants in Equation 4.24 correctly simplify to the totally specular and totally diffuse equations for isolated materials as derived in the Appendix. Similarly, case (c) simplifies to the specular case for a single material. The explicit solutions of Equation 4.24 are also shown in the Appendix.

Of particular interest is case (d), which represents a highly disordered limit for the support material with an atomically smooth interface and an exchange of phonons across the interface. In this limit, the distribution functions in Equation 4.22 reduce to

$$g_1^+(y,\theta_1) = \left[\frac{T_{12}}{1-(1-T_{12})\exp\left(\frac{d}{\tau_1 v_1 cos\theta_1}\right)} exp\left(-\frac{y}{\tau_1 v_1 cos\theta_1}\right) - 1\right] S_{o1}$$

$$g_1^-(y,\theta_1) = \left[\frac{T_{12}}{1-(1-T_{12})exp\left(\frac{d}{\tau_1 v_1 cos\theta_1}\right)} exp\left(\frac{d-y}{\tau_1 v_1 cos\theta_1}\right) - 1\right] S_{o1}$$

$$g_2^+(y,\theta_2) = g_2^-(y,\theta_2) = 0 \qquad \textbf{Equation 4.25}$$

Equation 4.25 shows that for increasing transmission or leakage of phonons from the graphene side to the support side, the distribution function approaches the totally diffuse case. Conversely, when transmission goes to 0, the graphene distribution function approaches the totally specular limit. Therefore, even for an atomically smooth and perfectly specular interface, highly disordered substrates behave as diffusely scattering boundaries in supported graphene. Figure 4.10 shows the expected heat flux profile from Equation 4.25 for different support materials. For decreasing τ_2, the substrate impedes heat flow in the supported MLG and approaches the case of isolated graphene with diffusely scattering boundaries in the limit $\tau_2 = 0$.

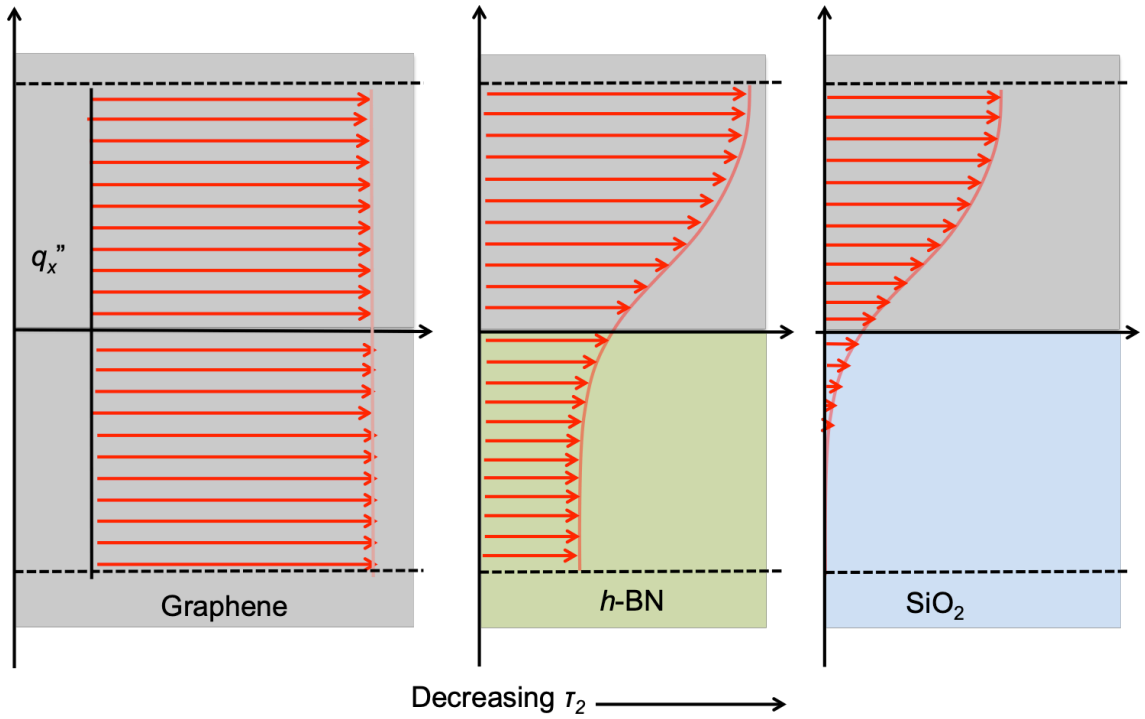

Figure 4.10: Heat flux profiles for a specular interface between the MLG and its support. For decreasing τ_2, the heat flux in the graphene approaches that of the isolated graphene case with diffusely scattering boundary conditions.

Finally, we note that the room temperature thermal conductivity of the 11-layer encapsulated sample of this study was between that of an 8-layer, clean and suspended sample and the 8-layer oxide supported sample by Sadeghi,[104] which are qualitatively similar to limiting cases (a) and (b), respectively.

4.6 Summary

A suspended micro-thermometry device was used to measure the thermal conductivity of a clean dry-transferred 11-layer MLG sample encased in *h*-BN. The results showed an increased thermal conductivity compared to a similar thickness MLG sample exfoliated from the same source but supported by SiO_2. Furthermore, in the low-

temperature limit where low-frequency phonons dominate thermal transport, the thermal conductivity was larger than an oxide-supported sample with three times its thickness. The role of intrinsic defects, lateral edge scattering, and dispersion relation alteration were discussed. Importantly, the extrinsic effect of the support substrate due to phonon leakage across the interface was investigated closely. The improved thermal transport is attributed to a lesser influence of phonon leakage from the MLG to the *h*-BN than to the oxide and, to some degree, reduced surface roughness. A solution of the BTE in the relaxation time approximation suggests that highly disordered support materials with vanishing τ can destroy the forward momentum of phonons in graphene even when the interface is atomically smooth.

Chapter 5: Conclusion

Owing to its ultrahigh thermal conductivity, graphene has received interest as a thermal management material for micro and nanoscale systems. Because of its atomic thickness, however, the degree to which graphene can spread heat from hot spots and redistribute their thermal profile remained uncertain. As a result, it had been suggested that increasing vertical heat transfer by increasing the interface conductance between graphene and its substrate could be a more important dissipation pathway to pursue. Furthermore, while theoretical studies have previously shown that an *h*-BN support could reduce the suppression of κ that was seen in SiO_2 supported graphene, there had hitherto been no experimental data to support the numerical predictions. This work has answered these critical questions regarding the thermal use of graphene, *h*-BN, and their heterostructure stack. The experimental findings and analytical models derived herein contribute to the fundamental understanding of heat transport at the micron and nanoscale and act as a guide for the rational design of graphene-based electronic devices.

Scanning thermal microscopy was used to visualize and quantify the temperature distribution of a large hot-spot in CVD-grown graphene under an electric bias. Electrostatic force microscopy revealed that the unusually large magnitude of the hot-spot was due to a rip near the center of the graphene strip, which is common in PMMA transferred 2-D materials. In turn, the rip formed a constricted channel region in the graphene, which significantly increased the current density near the defect. A coupled electro-thermal numerical model was built to simulate the experimental work, which showed good agreement with the measurement data for literature values of graphene thermal conductivity and interface conductance. Finally, an analytical model was derived

in an effort to better understand the competing effects of the lateral and vertical heat dissipation pathways and their dependence on κ and G, respectively. The study revealed that in substrates where the thermal spreading resistance of the support was much larger than the thermal interface resistance, increasing G did not reduce operating temperatures by any appreciable amount. Conversely, increasing the basal-plane thermal conductivity significantly reduces hot-spot magnitudes due to an increased heat spreading length of the graphene. Importantly, lateral spreading was shown to be effective even if the heat is not spread far enough to reach the nearby metal contacts. Instead, heat spreading counter-intuitively facilitates more efficient vertical dissipation by increasing the heat transfer area.

The results of the first study showed that to improve the thermal performance of thermally-thick substrates such as those proposed for flexible electronic platforms, it is imperative to increase lateral heat-spreading. To this end, the effect of adding a high-thermal conductivity *h*-BN interfacial layer between graphene and its substrate was studied using SThM. Two representative substrates were considered: (1) a Si substrate with 300 nm of SiO_2 and (2) a 100 μm thick flexible Corning Willow Glass substrate. The thermal images showed a clear formation of discrete hot spots in both devices when *h*-BN was not present. For equivalent power densities, the hot spot temperature in the graphene channel on Willow Glass was an order of magnitude larger than that on SiO_2/Si. Furthermore, because of its large thickness and low thermal conductivity, the WG temperature remained elevated even 20 μm away from the graphene edge. In contrast, nearly purely vertical dissipation through the relatively thin oxide was imaged on the Si substrate. When *h*-BN was included as an interface material, no well-defined hot spots

were observed in either the WG or SiO_2/Si devices. Instead, the measured profiles appeared to be blended, smooth and reduced in magnitude. An 80 nm thick *h*-BN layer between SiO_2/Si and graphene reduced the effective thermal resistance of the device by a factor of 2, while a 35 nm thick *h*-BN on WG showed a reduction in R_{th} by a factor of 4. An analytical model treating the graphene/*h*-BN stack as a combined heat fin showed good agreement with the experimental data. The analysis also revealed that the heat spreading length on thermally thick substrates scales with the heated area, which suggests *h*-BN can be an effective heat spreader even for few-micron wide hot-spots. The results conclude that inclusion of hexagonal boron nitride as a dielectric support for graphene can significantly reduce operating temperatures in microelectronic devices fabricated on low-thermal conductivity substrates.

More than a passive thermal interface material, the final study in this work showed that compared to an oxide substrate, an *h*-BN support improves the thermal conductivity of multilayer graphene. The maximum graphene thermal conductivity of the *h*-BN/graphene/*h*-BN hetereostructure was measured to be $996 \pm {}^{101}/_{47}$ W m^{-1} K^{-1}, compared to 820 W m^{-1} K^{-1} for a similar thickness MLG sample supported on oxide with one free surface. Furthermore, the peak graphene thermal conductivity was shifted to 200 K on *h*-BN compared to ~250 K for the oxide supported sample, which suggests a lesser influence of extrinsic phonon scattering mechanisms at the interface. The results can be explained by a super-lattice model, where thermal transport in the graphene is affected by interface surface roughness, transmission, and the nature of the substrate. To illustrate the effects of a highly disordered substrate on phonon transport, an analytical model for the heat flux in graphene was derived from the solution of the Boltzmann

transport equation in the relaxation time approximation. In an amorphous substrate where the relaxation time goes to zero, the support material behaves like a diffusely scattering boundary even when an atomically smooth and totally specular interface is imposed. In other words, in the specular limit, phonon scattering can still be affected by randomly oriented phonons arising from the amorphous substrate. On the other hand, due to its similar phonon dispersion and crystal structure compared to graphene and high phonon life tme, the phonons emerging from the *h*-BN support may maintain a larger degree of forward momentum similar to those leaving the adjacent MLG, which can explain the higher measured graphene thermal conductivity.

Appendix

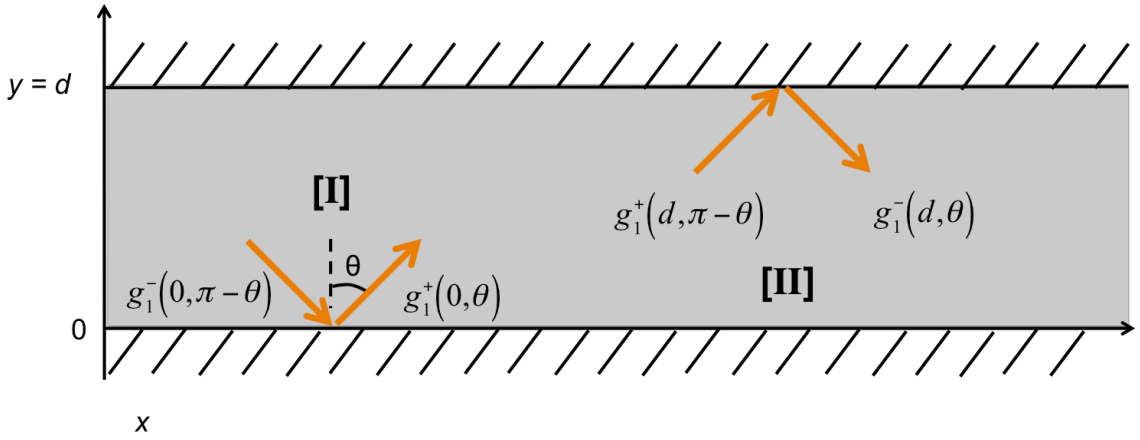

Figure A.1: Coordinate system used in solving the Boltzmann transport equation for an isolated material with partially diffuse, partially specular boundaries.

The coordinate system used to solve the BTE for a single, isolated material with partially specular, partially diffuse boundary conditions is shown in Figure A.1. The general solution for the distribution function is

$$g^+(y,\theta) = C^+ exp\left(-\frac{y}{\tau v cos\theta}\right) - S_o$$

$$g^-(y,\theta) = C^- exp\left(-\frac{y}{\tau v cos\theta}\right) - S_o \qquad \textbf{Equation A.1}$$

where g^+ is valid for phonons travelling in the positive x-direction such that $0 < \theta < \frac{\pi}{2}$ and g^- applies to phonons moving in the negative x-direction such that $\frac{\pi}{2} < \theta < \pi$. The boundary conditions for Equation A.1 are

$$[I]\ g^+(0,\theta) = Pg^-(0,\pi-\theta)$$

$$[II]\ g^-(d,\theta) = Pg^+(d,\pi-\theta)$$

for which the constants of integration are solved and substituted into Equation A.1 to give the general solution for the distribution function in the two regimes

$$g^+(y,\theta) = \left[\frac{S_o(1-P^2)P}{exp\left(-\frac{d}{\tau v cos\theta}\right) - P^2 exp\left(\frac{d}{\tau v cos\theta}\right)} - S_o(P-1)\right] exp\left(-\frac{y}{\tau v cos\theta}\right) - S_o$$

$$g^-(y,\theta) = \left[\frac{S_o(1-P^2)P}{exp\left(-\frac{d}{\tau v cos\theta}\right) - P^2 exp\left(\frac{d}{\tau v cos\theta}\right)}\right] exp\left(-\frac{y}{\tau v cos\theta}\right) - S_o$$

Equation A.2

For the totally diffuse case where P = 0, the solution for the distribution function simplifies to

$$g^+(y,\theta) = \left[exp\left(-\frac{y}{\tau v cos\theta}\right) - 1\right] S_o$$

$$g^-(y,\theta) = \left[exp\left(\frac{d-y}{\tau v cos\theta}\right) - 1\right] S_o$$

For the totally specular case where P = 1, the solution for the distribution function simplifies to

$$g^+(y,\theta) = g^-(y,\theta) = -S_o$$

The expected heat flux profiles in the graphene as given by Equation A.2 are shown in Figure A.2.

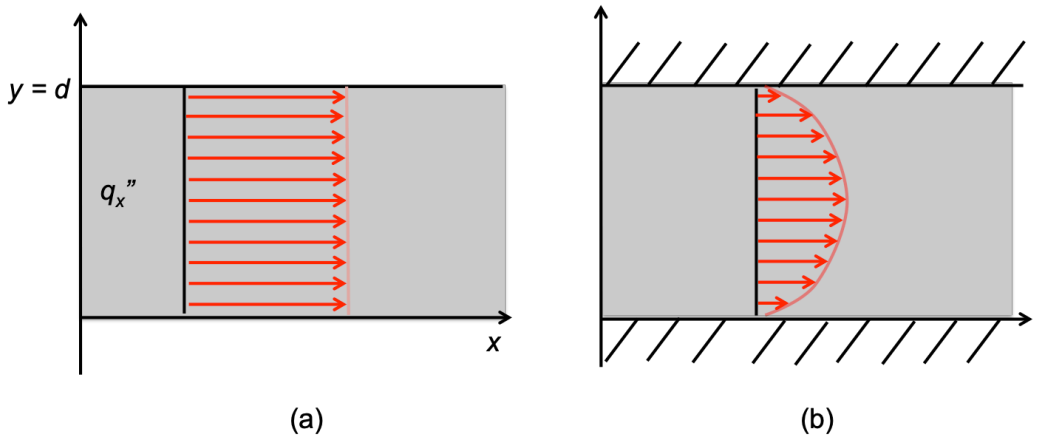

Figure A.2: Expected heat flux profiles in an isolated MLG sample for the limiting cases of (a) totally specular boundaries with *P = 1* and (b) diffusely scattering boundaries with *P = 0*.

The constants of integration for the superlattice structure in Equation 4.24 can be solved explicitly as

$$C_1^+ = \left[\frac{(\alpha_2\beta_1 + 1)S_{o1} + (\alpha_2 + \beta_2)S_{o2}}{1 - \alpha_1\alpha_2}\right] exp\left(-\frac{d}{\tau_1 v_1 cos\theta_1}\right)$$

$$C_1^- = \frac{(\alpha_2\beta_1 + 1)S_{o1} + (\alpha_2 + \beta_2)S_{o2}}{1 - \alpha_1\alpha_2}$$

$$C_2^+ = \frac{(\alpha_1 + \beta_1)S_{o1} + (\alpha_1\beta_2 + 1)S_{o2}}{1 - \alpha_1\alpha_2}$$

$$C_2^- = \left[\frac{(\alpha_1 + \beta_1)S_{o1} + (\alpha_1\beta_2 + 1)S_{o2}}{1 - \alpha_1\alpha_2}\right] exp\left(\frac{D}{\tau_2 v_2 cos\theta_2}\right)$$

where the coefficients α_i and β_i are defined as

$$\alpha_1 \equiv \frac{exp\left(-\frac{d}{\tau_1 v_1 cos\theta_1}\right) - (1 - T_{12})P_{1R}}{T_{21}P_{2T}}$$

$$\beta_1 \equiv \frac{(1 - T_{12})P_{1R} - 1}{T_{21}P_{2T}}$$

$$\alpha_2 \equiv \frac{exp\left(\frac{D}{\tau_2 v_2 cos\theta_2}\right) - (1 - T_{21})P_{2R}}{T_{12}P_{1T}}$$

$$\beta_2 \equiv \frac{(1 - T_{21})P_{2R} - 1}{T_{12}P_{1T}}$$

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